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THESIS

STRAY INSENSITIVE
SWITCHED CAPACITOR
COMPOSITE OPERATIONAL AMPLIFIERS

by

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In this research, analog active circuits are designed combining the properties of switched capacitors and composite operational amplifiers. This combined design improves upon the single operational amplifier's finite dc gain, smaller bandwidth, lower slew rate, finite input impedance and less than ideal output performance. The switched capacitor is implemented using both the toggle switch capacitor and the modifed open-circuit floating resistor techniques. The composite operational amplifier is implemented using the C2OA-1 and C2OA-2 designs from the CNOA-i possibilities. These four designs are evaluated in a finite-gain circuit and their results are compared with the results obtained from the continuous circuits of the same design.

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Stray Insensitive
Switched Capacitor
Composite Operational Amplifiers

by

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ABSTRACT

In this research, analog active circuits are designed combining the properties of switched capacitors and composite operational amplifiers. This combined design improves upon the single operational amplifier's finite dc gain, smaller bandwidth, lower slew rate, finite input impedance, and less than ideal output impedance. The switched capacitor is implemented using both the toggle switched capacitor and the modified open-circuit floating resistor techniques. The composite operational amplifier is implemented using the C2OA-1 and C2OA-2 designs from the CNOA-1 possibilites. These four designs are evaluated in a finite-gain circuit and their results are compared with the results obtained from the continuous circuits of the same design.

TABLE OF CONTENTS

I. INTRODUCTION

A. OVERVIEW

The operational amplifier (OA) is the most important analog integrated circuit today It is used in most all electronic designs Though the OA has a widespread use throughout the industry, the OA is not without its limitations An OA, by definition, is a lesson in compromise, speed is traded for accuracy, accuracy is traded for bandwidth, etc

The composite operational amplifier (CNOA-*i*) is a circuit with great flexibility It will improve the bandwidth, sensitivity, accuracy, and speed over the single OA

The switched capacitor network will decrease the size and improve the accuracy of component values during manufacturing This size reduction and increased accuracy will allow more designs to be implemented on a single integrated circuit (IC) than is possible otherwise

Combining the composite operational amplifier with parasitic free switched capacitor technology will produce an OA that has a considerable performance improvement and bandwidth extension over the single OA This combination has direct applications in A D and D/A conversion, digital communications, filtering, signal processing, speech processing, modulator-demodulator circuitry, HDTV, and neural network implementation to name a few

This thesis proposes to combine the composite operational amplifier and the switched capacitor network into a single stray insensitive design This new design should

produce an OA with an increased bandwidth and a decrease in sensitivity to both passive and active elements The removal of continuous resistors in the circuit using switched capacitors will decrease the area needed to implement this design on an IC

B. EXISTING PROBLEMS AND SOLUTIONS

The accuracy of the switched capacitor network can be degraded by the inherent and unpredictable error caused by parasitic capacitances found in an IC Two parasitic free, switched capacitor topologies, the Toggle Switched Capacitor (TSC) and the modified Open-circuit Floating Resistor (mOFR), provide a means to eliminate these stray capacitances

C. THESIS ORGANIZATION

The goal of this thesis is to implement a stray insensitive switch capacitor composite operational amplifier The operational amplifier will be discussed in the second chapter Composite operational amplifiers will be discussed in the third chapter Switched capacitor networks will be discussed in the fourth chapter Stray insensitive (parasitic free) switch capacitor networks will be discussed in the fifth chapter The sixth chapter will pictorially display the ten step process utilized in the development of the four designs used in this thesis. The seventh chapter contains the schematics for the four designs and it includes the experimental results obtained from those same four designs The eighth chapter will draw the necessary conclusions and will develop ideas for future research.

II. OPERATIONAL AMPLIFIERS

A. IN THE BEGINNING

During the 1950's the first operational amplifiers (OAs) began to appear, they were made from vacuum tubes, were larger than a breadbox, emanated more heat than a small furnace, and required large power supplies. More importantly, however, they were both unreliable and expensive.

The early 1960's brought about the transistor and solid state circuits and for the first time reliability was added to the operational amplifier equation.

The 1960's also brought about the space race. One of the many technological advances that resulted from this race to space was the development of the integrated circuit. By 1965 a commercially available integrated operational amplifier appeared - the Fairchild μA709.

Today OAs can be purchased in no less than 150 different types for specific applications as needed.

B. WHY THE OPERATIONAL AMPLIFIER

The widespread use of the OA can be traced to the ease of understanding its parts The OA behaves so much like its ideal characteristics that it is easy to comprehend and thus easy to implement in a design. With so many different OAs available there is a good chance that one already exists that will meet your design requirements

C. LIMITATIONS OF THE OPERATIONAL AMPLIFIER

The OA is a voltage controlled voltage source. The ideal OA has infinite input impedance, zero output impedance and infinite voltage gain. Designs using the op amp are too numerous to mention. Electronic designers have gone to great lengths to maximize the OAs strengths in their designs as well as work around their inherent weaknesses. The OA itself is quite a robust building block that has limitations such as finite dc gain, limited bandwidth, slow slew rate, finite input impedance, and less than ideal output resistance.

The differences between an ideal and a practical OA are many, in the next eight subsections a few of the differences that do exist will be touched upon as they have far reaching effects later on in this thesis.

1. Finite DC Gain

Ideal OAs have infinite gain, however, practical OAs have a more modest gain, typically in the range from 100 to 1 million.

2. Limited Bandwidth

An ideal OA has unlimited gain across the entire bandwidth (BW) Practical OAs have a limited useable bandwidth. As frequency increases the gain decreases due stray capacitances and finite carrier mobility. Additionally, internally compensated OAs have a 6 dB per octave gain rolloff due to the pole created by the compensating capacitor This 20 dB per decade rolloff will reduce an OA's gain from typically 100 dB at 10 Hz to 0 dB typically somewhere between 1 and 10 MHz.

3. Slew Rate

Slew rate is a limiting factor in practical OAs, ideal OAs are not slew rate limited. If a large input step voltage is applied to the input of a practical OA, some of the transistors in the OA might be driven out of their saturation regions, or possibly completely cut off. Therefore the OA output can no longer follow the applied input voltage at the same rate at which it was applied. The maximum rate of change that an OA can effectively transfer to its output is called the slew rate. Typically slew rate is in the few volts per micro second range.

4. Finite Input Impedance

The input impedance of an ideal OA is infinite. The input impedance of a practical OA is typically in the low MΩ range.

5. Nonzero Output Impedance

OAs with a buffering output stage have a nonzero output resistance typically up to a few kΩ, which prevents the OA from operating as an ideal voltage source This also limits the speed with which an OA can charge a capacitor connected to its output which, in effect, determines the highest useable signal frequency

6. Finite Linear Range

The output of a practical OA is determined by the difference between the input voltages multiplied by the gain of the OA, however this relationship only holds for a limited range of output voltage. The maximum value for the output voltage is usually

limited to the maximum dc supply voltage applied, or even a few volts less. Thus, with an applied dc voltage of ± 15 volts the output voltage might be limited to ± 12 volts.

7. Offset Voltage

An ideal OA whose inputs are tied together will produce an output voltage of zero volts. In a practical OA with the inputs tied together there will still be some voltage differential at the inputs which will be magnified by the gain at the output. The voltage needed to be applied to the OA to null the output voltage is called the offset voltage.

8. Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of a practical OA is a measure of how much the OA can suppress common-mode signals at the inputs. This allows the OA to suppress noise at its inputs if the CMRR is high. It is not uncommon to have a rejection in the range of 60-100 dB.

D. COMPOSITE OPERATIONAL AMPLIFIERS

The gain bandwidth product, the product of the finite gain of the OA and the 3dB frequency, is generally considered to be constant in a given OA. Speed, determined by slew rate limitations, and accuracy, determined by the input offset voltage, are usually not a variable that can be adjusted in single OA designs. However, there exists designs of multiple OAs that will allow for greater user control over these same characteristics

Composite OAs effectively extend the range of single OAs and lessen the impact of the single OA limitations. Chapter III will discuss this in some detail.

III. COMPOSITE OPERATIONAL AMPLIFIERS

A. THE NEED FOR THE COMPOSITE OPERATIONAL AMPLIFIER

Composite Operational Amplifiers (CNOAs) were developed by S. N. Michael and W. B. Mikhael in 1981, their research and its applications have been published in References 1 - 7. Their initial focus and subsequent development of CNOAs provided a systematic technique for extending the operational frequency range (bandwidth) of linear active networks. Active compensation was examined and applied to the design of active filter networks.

The systematic technique for extending the bandwidth (BW) using CNOAs originated from using the nullator-norator pairing to create 136 possible circuit designs that were then subjected to the following performance criteria:

1. The noninverting and inverting open-loop gains of each of the 136 C2OAs should show no change in sign in the denominator polynomial coefficients. This satisfies the necessary, but not sufficient, conditions for stability. Also, none of the numerator or denominator coefficients of the noninverting and inverting polynomial coefficients should be realized through differences. This eliminates the need for single op amps with matched GBWPs and results in low sensitivity of the C2OA with respect to its components.

2. The external three-terminal performance of the C2OA should resemble, as closely as possible, the three-terminal performance of the single OA.

3. To minimize phase shifts no right-half *s*-plane (RHS) zeros due to the single OA pole were allowed in the closed-loop gains of the C2OAs.

4. To justify the increased number of OAs, the C2OA had to have an extended frequency operation with minimum gain and phase deviation from the ideal transfer function.

B. THE THEORY BEHIND THE COMPOSITE OPERATIONAL AMPLIFIER

An operational amplifier is a voltage controlled voltage source (VCVS). In the ideal case the input impedance, Z_{in}, would approach infinity, the output impedance, Z_{out}, would approach 0, and the open loop gain, A, would approach infinity. This can be directly transferred to the idealized model using nullator and norator singular elements [Refs. 2,4]. A nullator is a one port which neither sustains a voltage nor passes a current. A norator is a one port which will sustain an arbitrary voltage and pass an arbitrary independent current [Refs. 1,4]. These models can be seen in Figure 3.1. Using the nullator-norator method of analysis CNOAs (where N = 2) were developed. Only four of the original 136 possible designs met all four of the above performance criteria, they are numbered C2OA-1 through C2OA-4. The resulting composite devices had three external terminals which resembled the input and output terminals of a single op amp.

The single pole model open-loop gain of the single OAs used in the modeling of the C2OAs is

$$A_i = \frac{A_{oi}\omega_{Li}}{\omega_{Li}+S} = \frac{\omega_i}{S+\omega_{Li}} , \quad i = 1 \text{ or } 2 \tag{3.1}$$

where A_{oi} , ω_{Li} , and ω_i are the dc open-loop gain, the 3dB bandwidth, and the gain bandwidth product (GBWP) of the ith single OA, respectfully. The open-loop input-output relationships for the C2OA-1 through C2OA-4 can be described by

$$V_{oi} = V_a A_{ai}(S) - V_b A_{bi}(S) , \quad i = 1 \ldots 4 \tag{3.2}$$

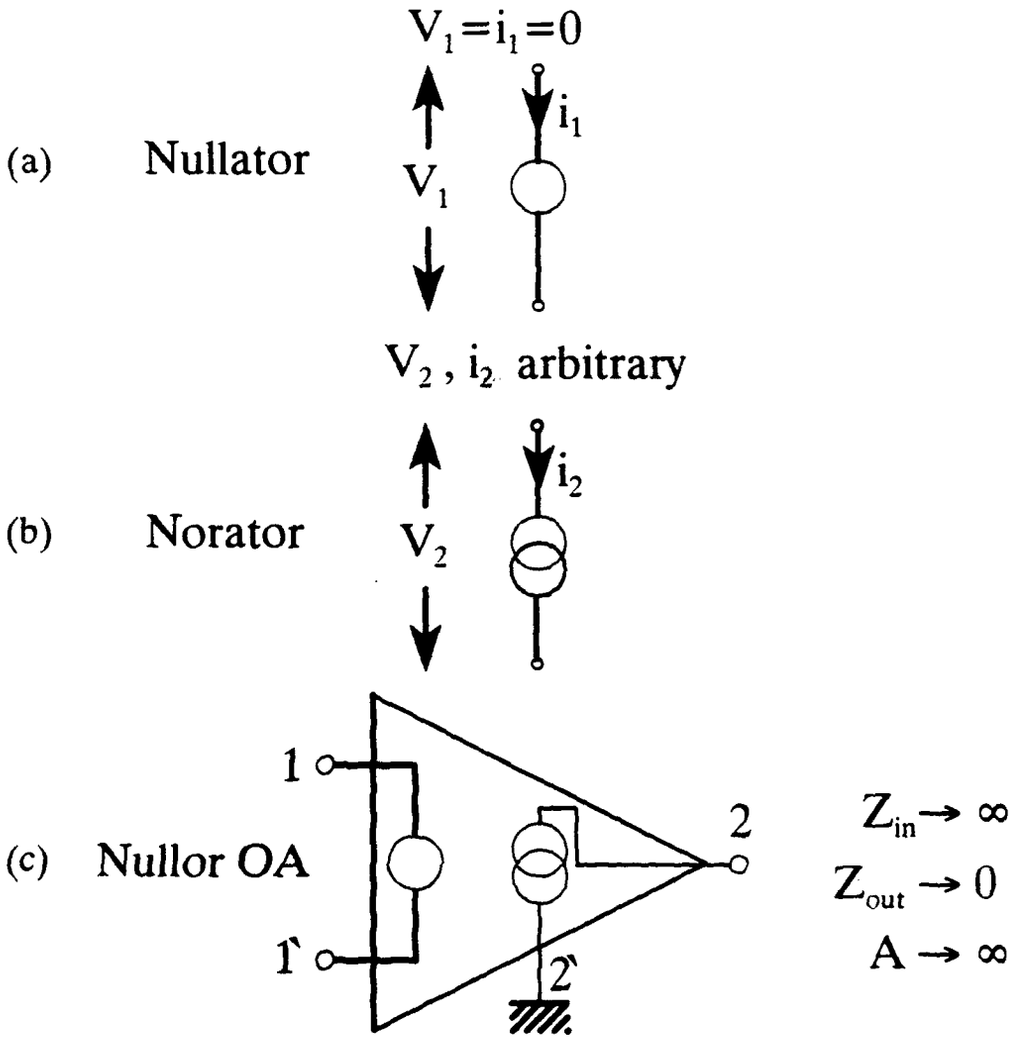

Figure 3.1 (a) Nullator, (b) Norator, (c) Nullor OA (VCVS)

C. C2OA-1

For C2OA-1 the open-loop gain input-output relationship can be derived from Equation 3.2 as

$$V_{o1} = V_a \frac{A_2(1+A_1)(1+\alpha)}{A_1 + (1+\alpha)} - V_b \frac{A_1 A_2(1+\alpha)}{A_1 + (1+\alpha)} \tag{3.3}$$

where α is the internal resistor ratio as shown in Figure 3.2.

References 1, 2, and 3 derive the 3db frequency equation and Q equation to be

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1+k}} \tag{3.4}$$

$$Q_p = \frac{(1+\alpha)}{\sqrt{(1+k)}} \sqrt{\frac{\omega_2}{\omega_1}} \tag{3.5}$$

where α is the internal resistor ratio, ω_p is the 3db point, k is the closed-loop gain, ω_1 is the GBWP for A_1 , and ω_2 is the GBWP for A_2. The Routh-Hurwitz criterion produces the necessary and sufficient conditions for stability as

$$(1 + \alpha) < \frac{1 + k}{2} \tag{3.6}$$

The C2OA-1 in Figure 3.2 clearly shows the similarity of the three terminal configuration between the composite OA and that of a single OA. Inputs a and b are the noninverting and inverting inputs for the composite OA just as they would be on a single OA.

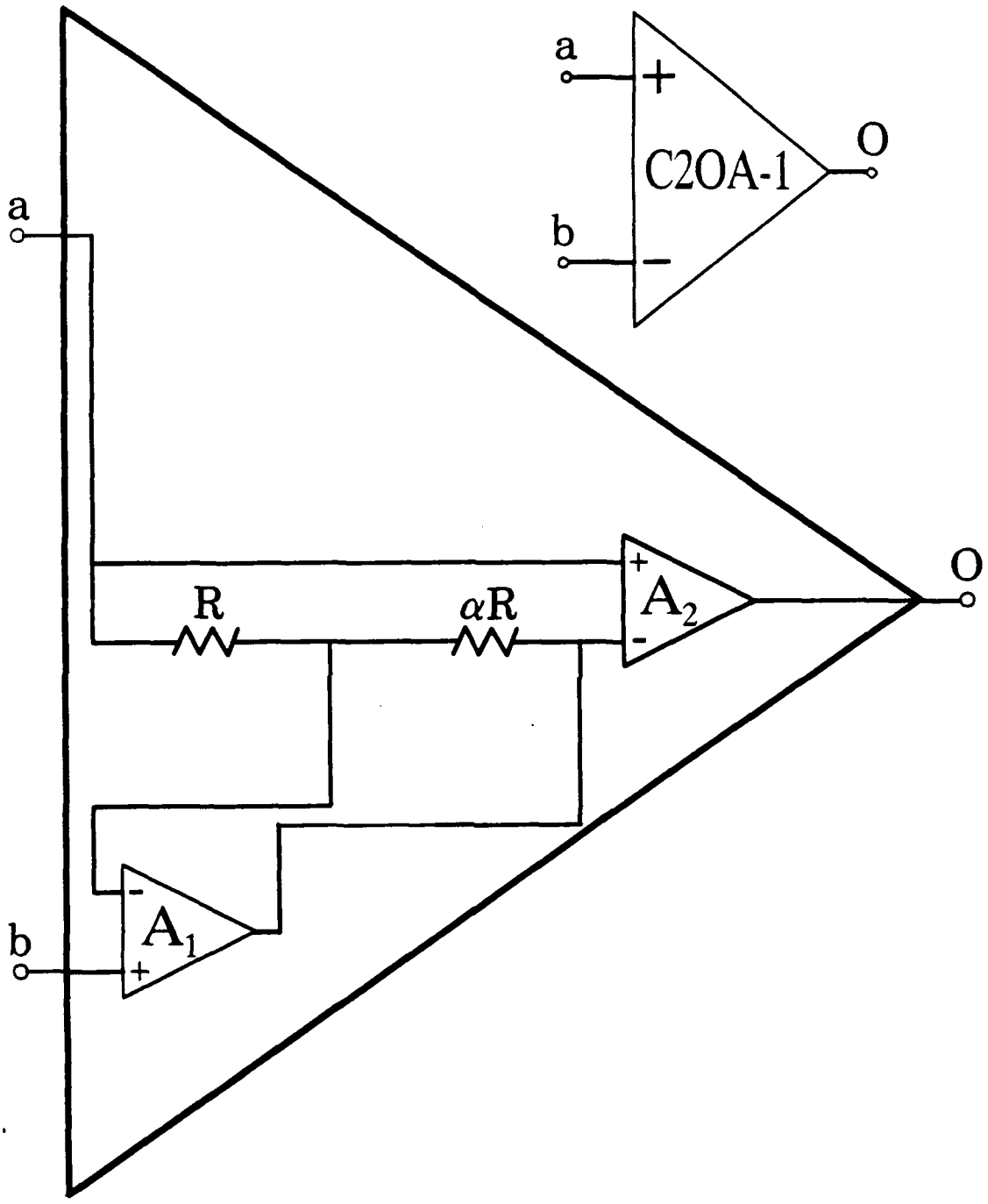

Figure 3.2 C20A-1

D. C2OA-2

For C2OA-2 the open-loop gain input-output relationship can be derived from Equation 3.2 as

$$V_{o2} = V_a \frac{A_1 A_2 (1+\alpha)}{A_2 + (1+\alpha)} - V_b \frac{A_1 A_2 (1+\alpha)}{A_2 + (1+\alpha)} \tag{3.7}$$

where α is the internal resistor ratio as shown in Figure 3.3.

References 1, 2, and 3 derive the 3db frequency equation and Q equation to be

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1+k}} \tag{3.8}$$

$$Q_p = \frac{(1+\alpha)}{\sqrt{(1+k)}} \sqrt{\frac{\omega_1}{\omega_2}} \tag{3.9}$$

where α is the internal resistor ratio, ω_p is the 3db point, k is the closed-loop gain, ω_1 is the GBWP for A_1 , and ω_2 is the GBWP for A_2. The Routh-Hurwitz criterion produces the necessary and sufficient conditions for stability as

$$(1 + \alpha) < \frac{1 + k}{2} \tag{3.10}$$

The C2OA-2 in Figure 3.3 clearly shows the similarity of the three terminal configuration between the composite OA and that of a single OA. Inputs a and b are the noninverting and inverting inputs for the composite OA just as they would be on a single OA.

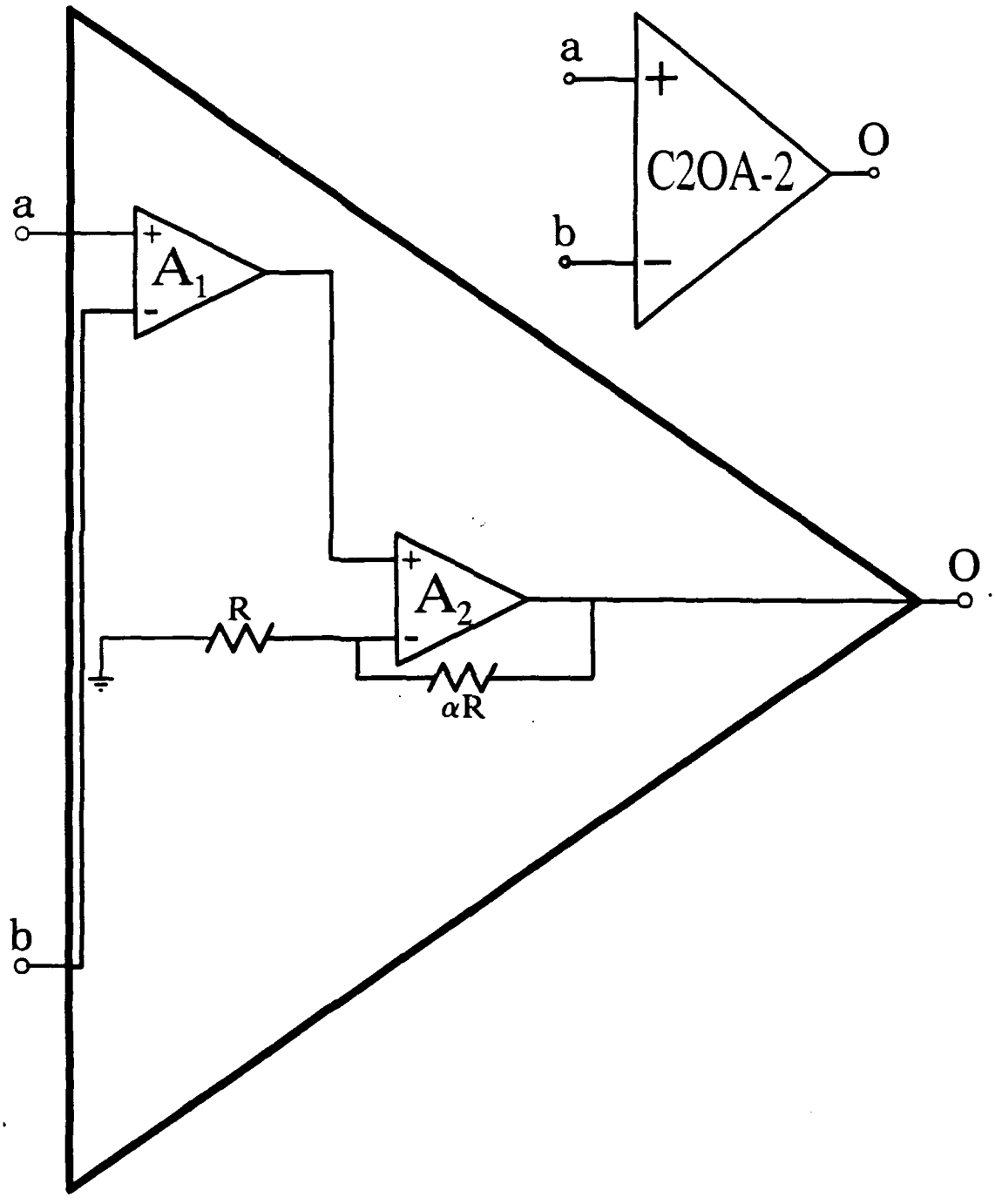

Figure 3.3 C2OA-2

E. C2OA-3

For C2OA-3 the open-loop gain input-output relationship can be derived from Equation 3 2 as

$$V_{o3} = V_a \frac{A_1 A_2}{(1+\alpha)} - V_b \frac{A_2(1+A_1)}{(1+\alpha)} \tag{3.11}$$

where α is the internal resistor ratio as shown in Figure 3.4.

References 1, 2, and 3 derive the 3db frequency equation and Q equation to be

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{(1+k)(1+\alpha)}} \tag{3.12}$$

$$Q_p = \sqrt{\frac{(1+k)(1+\alpha)\omega_1}{\omega_2}} \tag{3.13}$$

where α is the internal resistor ratio, ω_p is the 3db point, k is the closed-loop gain, ω_1 is the GBWP for A_1, and ω_2 is the GBWP for A_2. The Routh-Hurwitz criterion produces the necessary and sufficient conditions for stability as

$$(1 + \alpha) > \sqrt{1 + k} \tag{3.14}$$

The C2OA-3 in Figure 3.4 clearly shows the similarity of the three terminal configuration between the composite OA and that of a single OA. Inputs a and b are the noninverting and inverting inputs for the composite OA just as they would be on a single OA.

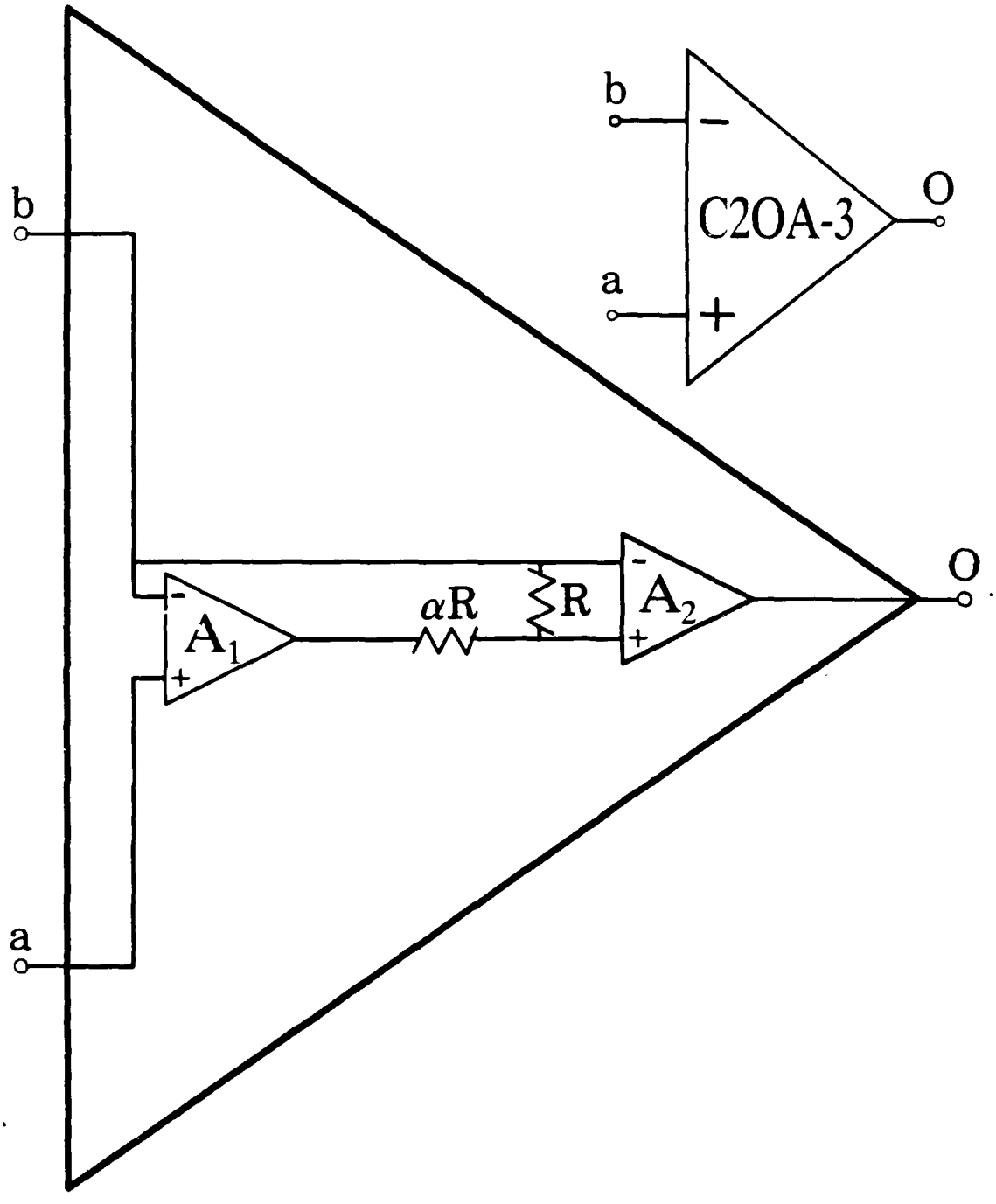

Figure 3.4 C2OA-3

F. C2OA-4

For C2OA-4 the open-loop gain input-output relationship can be derived from Equation 3.2 as

$$V_{o4} = V_a \frac{A_2(A_1+\alpha)}{(1+\alpha)} - V_b \frac{A_2\,[A_1 + (1+\alpha)]}{(1+\alpha)} \tag{3.15}$$

where α is the internal resistor ratio as shown in Figure 3.5.

References 1, 2, and 3 derive the 3db frequency equation and Q equation to be

$$\omega_p = \sqrt{\frac{\omega_1\omega_2}{(1+k)(1+\alpha)}} \tag{3.16}$$

$$Q_p = \sqrt{\frac{(1+k)\omega_1}{(1+\alpha)\omega_2}} \tag{3.17}$$

where α is the internal resistor ratio, ω_p is the 3db point, k is the closed-loop gain, ω_1 is the GBWP for A_1, and ω_2 is the GBWP for A_2. The Routh-Hurwitz criterion produces the necessary and sufficient conditions for stability as

$$(1 + \alpha) > 4(1 + k) \tag{3.18}$$

The C2OA-4 in Figure 3.5 clearly shows the similarity of the three terminal configuration between the composite OA and that of a single OA. Inputs a and b are the noninverting and inverting inputs for the composite OA just as they would be on a single OA.

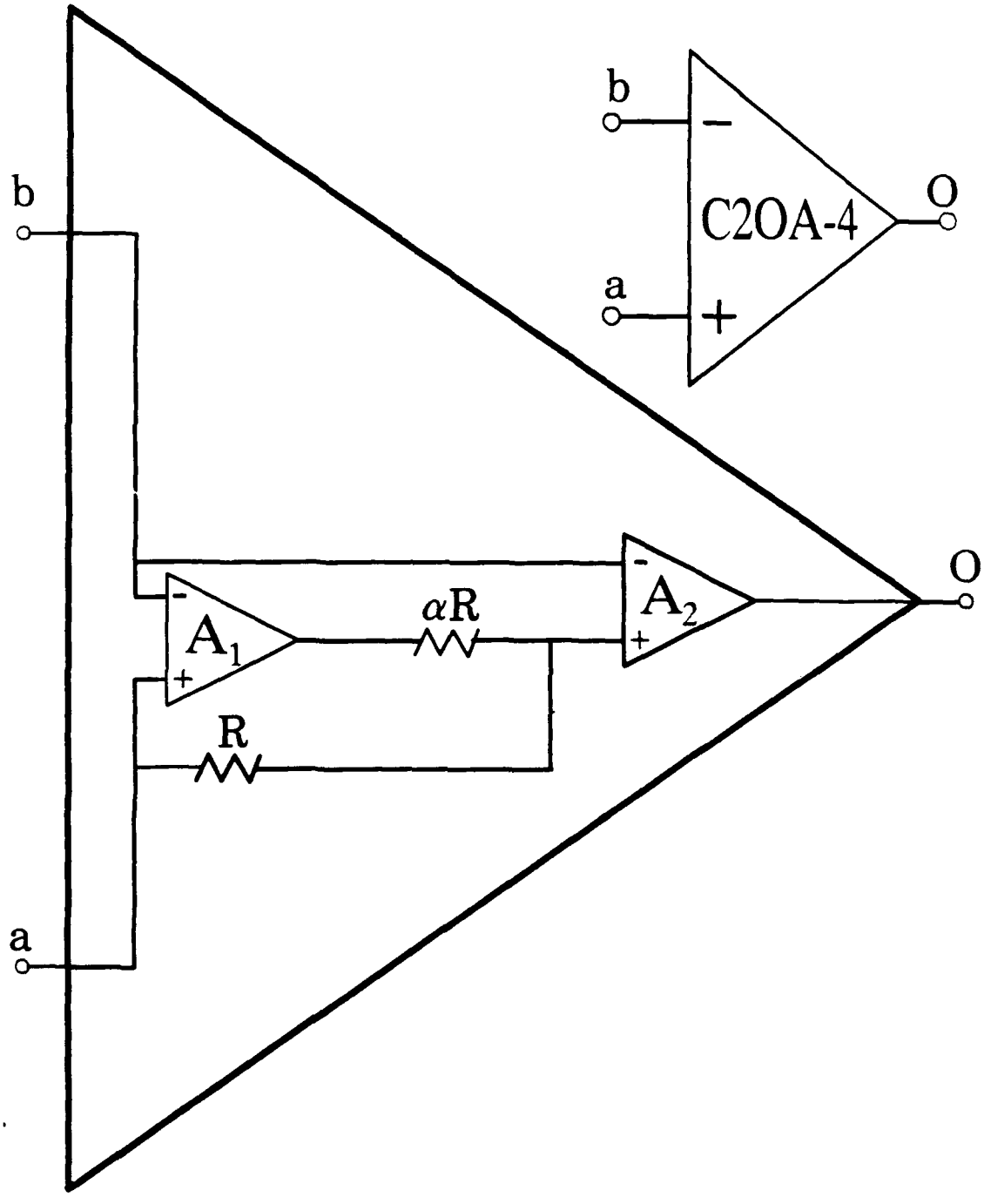

Figure 3.5 C2OA-4

G. ESTABLISHING ACCEPTABLE VALUES FOR α AND K

It should be noted that the 3db frequency equations (Equations 3.4, 3.8, 3.12, and 3.16), the Q equations (Equations 3.5, 3.9, 3.13, and 3.17), as well as the Routh-Hurwitz criterion equations (Equations 3.6, 3.10, 3.14, and 3.18) are all functions of the compensation resistor ratio α and the closed-loop gain k.

The closed-loop gain, k, can be controlled by the designer in many implementations (as in a finite-gain configuration) and this should allow for a great degree of freedom in obtaining an acceptable Q and ω_p for the desired design requirements. The compensation resistor ratio, α, can likewise be selected with a similar amount of freedom.

Thus for each of the four C2OAs it is quite easy to select theoretical values for k and α while ensuring that the required stability is maintained in each of the four implementations.

H. INCREASED BANDWIDTH WITH THE C2OAs

A single OA in a finite-gain amplifier configuration has a BW that decreases approximately by a factor of 1/k relative to its GBWP. When two OAs are cascaded together in a finite-gain amplifier configuration, the maximally flat, thus optimum, GBWP is obtained when each amplifier, A_1 and A_2, has an individual gain of $\sqrt{k}$, in order to realize an overall gain of k. The resulting BW shrinks by approximately $0.66 / \sqrt{k}$. The GBWP of C2OA-1 and C2OA-2 can be designed to shrink by only a factor of

$1 / \sqrt{K}$ for $Q_p = 0.707$ (maximally flat) [Ref. 4]. These theoretical BWs are shown more clearly in Figure 3.6.

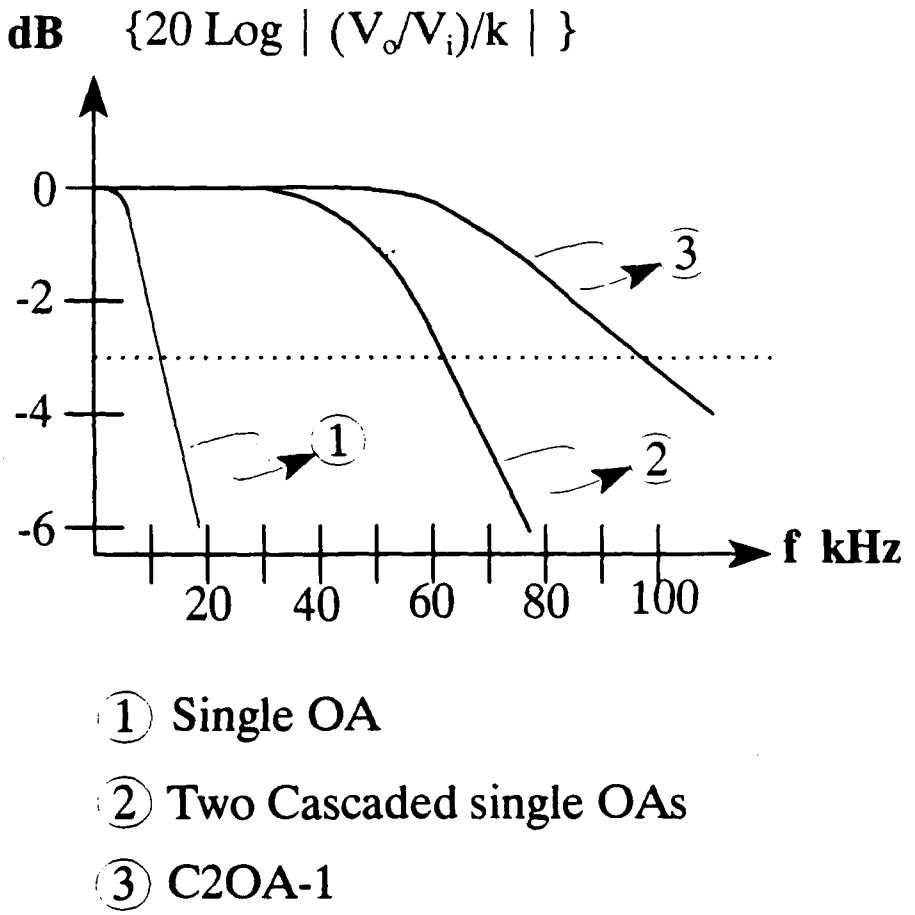

Figure 3.6 Theoretical responses of negative finite-gain amplifiers realized using Single OA, Two Cascaded Single OAs, and C2OA-1 for negative gain of 100, and GBWP = 1 MHz

I. SENSITIVITIES OF THE COMPOSITE OPERATIONAL AMPLIFIER

In addition to significant bandwidth improvements, the C2OA configuration also offers a decreased sensitivity to active and passive components. This is a direct result of the first performance criteria mentioned earlier in this chapter. The 3 dB frequency equations (Equations 3.4, 3.8, 3.12, and 3.16) and the Q equations (Equations 3.5, 3.9, 3.13, and 3.17) are functions of the GBWPs of the single OAs (A_1 and A_2) and α, the compensation resistor ratio in the composite OA.

The finite gain transfer functions for the C2OAs have the general form

$$\frac{1 + as}{1 + b_1 s + b_2 s^2} \tag{3.19}$$

where

$$b_1 = \frac{1}{\omega_p Q} \tag{3.20}$$

and

$$b_2 = \frac{1}{\omega_p^2} \tag{3.21}$$

Neither the a or b coefficients are realized through differences, this eliminates the need for single OAs with matched GBWPs and results in low sensitivity of the C2OA with respect to its components [Refs. 3, 4].

J. INPUT OUTPUT OFFSET VOLTAGES

Operational amplifiers typically have large gains and will amplify any voltage differential at its inputs. An ideal OA with both inputs grounded would have an output of zero volts. All OAs in the real world have a small DC voltage differential at the inputs referred to as the input offset voltage (V_{off}). This voltage when amplified by the gain of the amplifier is referred to as output offset voltage [Ref. 8:pp. 133 - 138]. This input voltage differential can be attributed to a voltage difference applied to the two inputs of the OA (ideal OAs), or it can be attributed to a voltage difference due to the transistor pairs in the input differential stage having different gains and different internal impedances [Ref. 8:pp. 500-504], or both (real world).

Input offset voltage places an artificial lower limit on the DC voltage that can be accurately detected and amplified. The smaller the offset voltage, the more accurately the OA can detect and amplify the input signal. Offset voltages are fairly small and normally are found in the few millivolt range. This small voltage differential at the inputs however will be amplified by the OA gain and could produce a degraded output signal. The possible solutions to voltage offset problems are many but the most common are to use an input bias resistor, or to simply select an OA with a smaller offset voltage. The problem with the former solution is that not all designs will allow a input bias resistor to be used and the later solution typically comes at a cost - a slower slew rate. The composite OA allows for yet another solution, select a small offset voltage OA for A_1 and select a high slew rate OA for A_2. This can more easily be shown from the values for V_{off} for composite OAs shown in Table 3.1. Notice that V_{off} is for all practical purposes

a function of V_{off1} alone and not of V_{off2}. For C2OA-2, C2OA-3, and C2OA-4 V_{off2} is divided by the open loop gain (A1) from OA A_1. This value (A1) will always be very large yielding an extremely small effect on the overall value of V_{off}. In the case of C2OA-1, as long as α remains relatively large then V_{off2} will not play a substantial part in the overall value of V_{off} either.

Table 3.1 C2OA INPUT OFFSET VOLTAGES

C2OA-*i*	Input Offset Voltages
C2OA-1	$V_{off} = V_{off1} + (V_{off2} / \alpha)$
C2OA-2	$V_{off} = V_{off1} + (V_{off2} / A1)$
C2OA-3	$V_{off} = V_{off1} + (V_{off2} (1 + \alpha) / A1)$
C2OA-4	$V_{off} = V_{off1} + (V_{off2} (1 + \alpha) / A1)$

K. SLEW RATES

Slew rate (SR) is the maximum possible rate of change of the OA output voltage [Ref. 8:p. 124]. Slew rate is dependent upon the bias current and the internal compensation capacitor value [Ref. 8:pp. 771 - 772]. A faster slew rate is preferable in most applications, however, a faster slew rate comes at the expense of an increase in input offset voltage. Most OA designs either incorporate a fast SR design or they incorporate a small offset voltage design.

The composite OA offers an alternative. It has already been shown that the offset voltage for a composite OA is determined by the A_1 op amp, thus, choosing an OA with

an extremely small offset voltage along with its distortion and dynamic range limitations, will not hinder the output of the composite op amp due to the composite's output being dependent upon the characteristics of the output op amp, A_2 [Refs. 1, 2, 9, 10].

The output op amp, A_2, can be chosen for its high slew rate, wide bandwidth, and fast settling time thus improving the overall performance of the composite OA. The composite OA can now be designed with a low offset voltage input stage and a high slew rate, wide bandwidth, fast settling output stage for superior performance, if needed.

L. SUMMARY

CNOAs can be made for any value of $N > 2$. The generation of C2OAs was shown in this chapter, but by simply replacing any single OA (A_1 or A_2) in a C2OA configuration with a C2OA will produce a C3OA. This method can by used for any value of N. Details of proven designs for $N > 2$ can be found in References 1 - 7.

The composite OA can be made to exacting design specifications by choosing the appropriate OAs for A_1 and A_2 and careful consideration of the value for α as well. If the C2OA cannot precisely meet any specification then a CNOA with $N > 2$ can easily be chosen to fill the need.

CNOAs have an extremely low sensitivity, a high GBWP, can be tailored to provide a low offset voltage and high slew rate and can handle the mismatch between the GBWPs of op amps A_1 and A_2.

IV. SWITCHED CAPACITOR NETWORKS

A. THE RC TIME CONSTANT

The RC time constant is the limiting factor in modern active filter design. Since resistors and capacitors are made in different steps in the fabrication process, their errors cannot not track one another. Additionally, the temperature and voltage coefficients of resistors and capacitors are not correlated; therefore, the time constants will always vary a little with temperature and signal level.

The obvious solution is to either make the time constant a factor solely of resistance or solely of capacitance, but not a combination of both. Capacitances can be made more accurately, at less expense, and they occupy a much smaller area on an integrated circuit than a resistor would. The choice then is obvious, replace the RC time constant with a constant c.

Frequency is determined by the RC time constant. We are looking for frequency to be set by the constant c in order to be more accurate and to save valuable real estate on an IC chip. Starting with the RC time constant we have

$$\omega_o = \frac{1}{RC} \tag{4.1}$$

Converting this expression to strictly a capacitive one leads to

$$\omega_o = c f_c = \frac{C_R}{C} f_c \qquad (4.2)$$

We use f_c to ensure that we have the correct units for ω_o which is 1/time. Substituting the expression for ω_o in Equation 4.2 into the variable ω_o in Equation 4.1 and subsequently solving for R yields

$$R = \frac{1}{f_c C_R} \qquad (4.3)$$

Equation 4.3 simply implies that a resistor can be replaced by a circuit that satisfies the above expression. The circuit or network that replaces the resistor and that satisfies this expression is called the switched capacitor (SC). The switched capacitor circuit is shown in Figure 4.1 below.

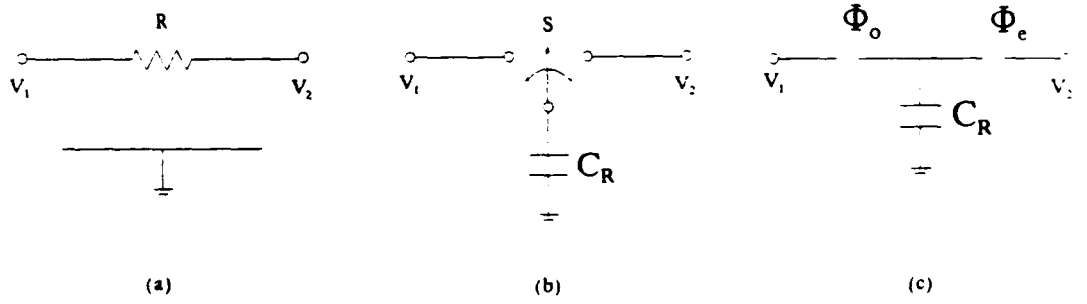

Figure 4.1 (a) Resistor, (b) Switched Capacitor equivalent, (c) Circuit Diagram

Figure 4.1a is generic resistor in a circuit that can be replaced by the circuit in Figure 4.1b, a generic switched capacitor equivalent circuit. Taking a closer look at Figure 4.1b we have capacitor C_R connected to the left node with voltage V_1, thus C_R stores charge

$$Q_1 = C_R V_1 \tag{4.4}$$

Subsequently connecting capacitor C_R to the right node with voltage V_2 it follows that

$$Q_2 = C_R V_2 \tag{4.5}$$

The charge that was actually transferred from V_1 to V_2 becomes

$$\Delta Q = Q_1 - Q_2 = C_R (V_1 - V_2) \tag{4.6}$$

The switching of C_R between the two nodes is handled by a switch, S, hence the name switched capacitor. The switch, S, can be flipped periodically with a clock period, T, such that the clock frequency can now be defined as $f_c = 1/T$. If f_c is kept sufficiently greater than the signal frequency, f, such that

$$f_c >> 2f \tag{4.7}$$

then the voltage sources V_1 and V_2 can be assumed to be constant over the period T.

The definition for current is

$$i = \frac{dq}{dt} \tag{4.8}$$

or on the average what we really have is

$$I \approx \frac{\Delta Q}{T} \tag{4.9}$$

but we had previously defined $f_c = 1/T$, so

$$I \approx \Delta Q f_c \tag{4.10}$$

it follows from Equation 4.6 that

$$I \approx f_c C_R (V_1 - V_2) \tag{4.11}$$

or by rearranging we have

$$\frac{1}{f_c C_R} = \frac{(V_1 - V_2)}{I} \tag{4.12}$$

recalling Equation 4.3 leaves us with

$$R \approx \frac{1}{f_c C_R} = \frac{(V_1 - V_2)}{I} \tag{4.13}$$

This derivation ends with Equation 4.13 which shows us that Figure 4.1a and Figure 4.1b are indeed approximately equivalent.

Figure 4.1c depicts the circuit equivalent of the switch capacitor. Here we have two nonoverlapping clock signals, Φ_o and Φ_e, to ensure that the capacitor is in fact switched between the two voltages without any possibility of both switches being closed at the same time. The two clock signals are generated from a single clock for the same reason This arrangement is best shown in Figure 4.2.

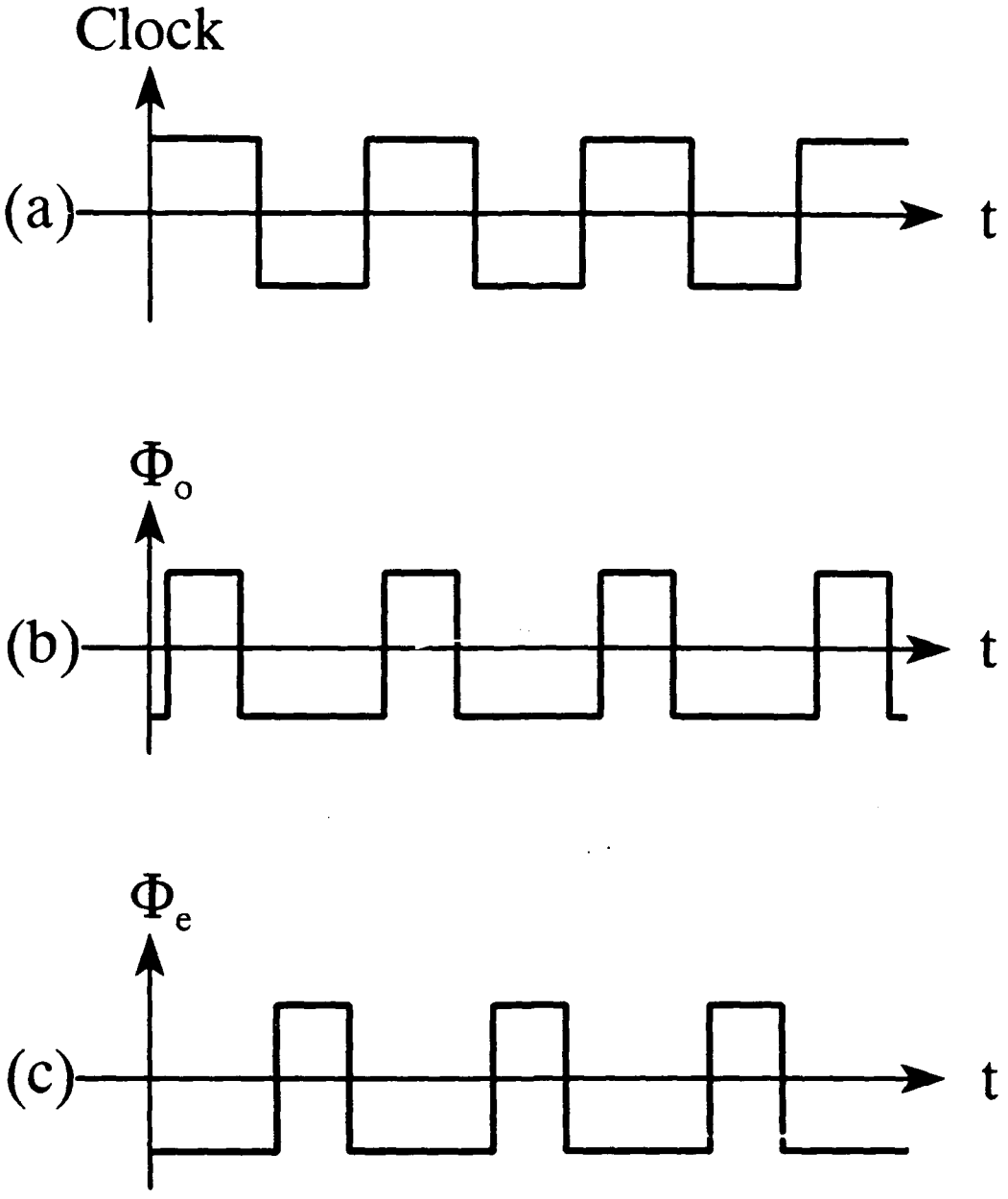

Figure 4.2 (a) Clock, (b) Odd Phase Clock Signal, (c) Even Phase Clock Signal

The switched capacitor implementation of the continuous resistor has solved the two most troublesome problems with the RC time constant namely that the frequency parameters are now set as a function of the ratio of two capacitors and a clock frequency

$$\tau_o = \frac{1}{\omega_o} = \frac{1}{f_c}\frac{C}{C_R} \qquad (4.14)$$

and that the required real estate on an IC has been reduced drastically. To give us some idea as to how much area was saved let's assume that C_R was 1pF in size. Using Equation 4.3 and a nominal frequency of 100 kHz results in an R value of 10 MΩ. The 1 pF capacitor will occupy a chip area of approximately 2500 μm^2 and the 10 MΩ resistor will occupy a chip area of approximately 10^6 μm^2. Thus the capacitor only requires a chip area of approximately 0.25% the area of the resistor it replaces.

B. TWO PHASE NONOVERLAPPING CLOCK

The two phase nonoverlapping clock requirement for a switched capacitor is easily implemented. Figure 4.3 shows a simple circuit that will produce a two phase nonoverlapping clock. It is this circuit that will be used in this thesis to produce the needed clocks. The input clock frequency, f_c, will be maintained sufficiently above the signal frequency, f, by using a signal frequency of 10 kHz and a clock frequency of 1 MHz.

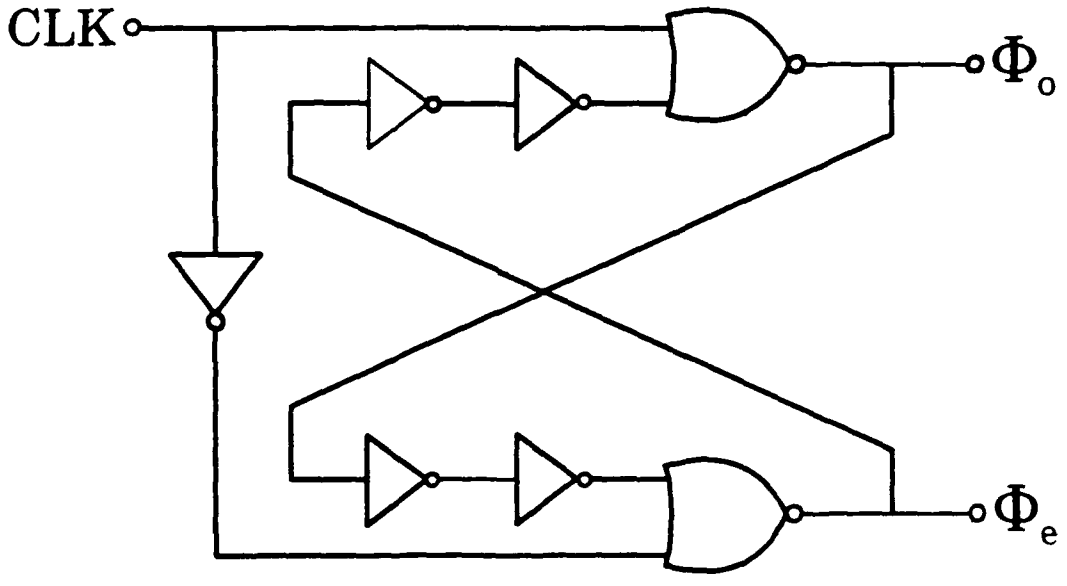

Figure 4.3 Circuit Diagram for a Two Phase Nonoverlapping Clock

C. NONIDEAL PROPERTIES OF SWITCHED CAPACITORS

The switched capacitor equivalent circuit shown in Figures 4.1b and 4.1c contain switches. These switches, when clocked, will produce some undesirable side effects, namely clock feed through. Clock feed through is one of four main challenges when using switched capacitor networks, the other three are:

1. Offset Error and Noise.
2. Nonlinear P-N Junction Capacitance.
3. Incomplete Transfer of Charge.

Offset error was discussed in Chapter III. Clock feed through, nonlinear P-N junction capacitance, and incomplete transfer of charge will be discussed in Chapter V.

D. SWITCHED CAPACITOR VERSUS DIGITAL IMPLEMENTATION

Switched capacitor networks and digital signal processors (DSPs) have advantages and disadvantages compared to one another depending upon the desired implementation. To always say that one is better than the other would be foolish indeed, however, the digital signal processor does possess some advantages over the switched capacitor network in some arenas.

The switched capacitor network disadvantages include:

1. Limited Accuracy.
2. Dynamic Range.
3. Flexibility and Programmability.
4. Nonstandard Microprocessor Technology.

1. Limited Accuracy

The ratio of capacitors that is so crucial to successful SC implementation is its biggest weakness. Currently, these capacitors can be accurately built to within a 0.1% tolerance of their nominal values. This is truly remarkable, however, this also equates to an approximate 10-bit floating point accuracy. This accuracy certainly would not be enough for applications requiring 16, 32, or even 64-bit accuracy.

2. Dynamic Range

The SC network requires the use of OAs and switches. It is this very combination that limits its dynamic range. There is a very large amount of noise in every SC network originating from the switches and the OAs. Add in the more modest noise from supply lines and the clock and we end up with a dynamic range that seldom ever exceeds 100 dB in the SC configuration and typically ranges in the 70 - 90 dB range. Digital signal processors maintain a much higher dynamic range.

3. Flexibility and Programmability

Switched capacitor circuits can be made programmable, however, the ease at which a digital signal processor can be made programmable and then have its characteristics changed simply by selecting different coefficients from a ROM will be hard to match any time soon.

4. Nonstandard Microprocessor Technology

Digital signal processors are built with the same technology that has been doubling our clock speeds and doubling our transistors per CPU every three years. There

is a concentrated and continuous effort to increase this technology even more and with it, so will DSPs see an increase in performance, accuracy, and flexibility.

All is not lost however, whenever simplicity, speed, limited IC real estate, small dc bias power are required or when the input or output signals are inherently analog in nature then switched capacitor implementation would be the preferred choice.

More often than not, what will be seen is the melting of the two technologies. The mixing of analog and digital in the same configuration is happening more and more today. Designers are trying to use the advantages of each in order to improve overall product.

As long as humans hear with analog ears then analog implementations will be required.

V. STRAY INSENSITIVE SWITCHED CAPACITOR NETWORKS

A. OVERVIEW

Switched capacitor networks require an accurate ratio of capacitors, α. This ratio provides the necessary time constant as well as the capacitance needed to replace the continuous resistor found in the original circuit. Currently capacitors can be made to achieve a ratio accuracy of about 0.1%. This accuracy in capacitor manufacturing provides the same comparative accuracy to the ratio of capacitors, α.

Practical capacitors are not ideal. Practical capacitors inherently have internal stray (parasitic) capacitances.

Additionally, switched capacitor circuits also have an inherent stray capacitance built into them. These parasitic capacitances are unpredictable and can significantly affect the performance of any switched capacitor network. The parasitic capacitances found in all switch capacitor networks cannot currently be eliminated, however, they can be made ineffective by using an appropriate switched capacitor topology.

B. STRAY CAPACITANCE IN THE MOS CAPACITOR

Figure 5.1 is a silicon realization of a MOS capacitor that has been redrawn from a similar figure found in Reference 11. In this case the MOS capacitor represents the capacitance C_R. This figure clearly shows the stray capacitances that are to be found in the MOS capacitor.

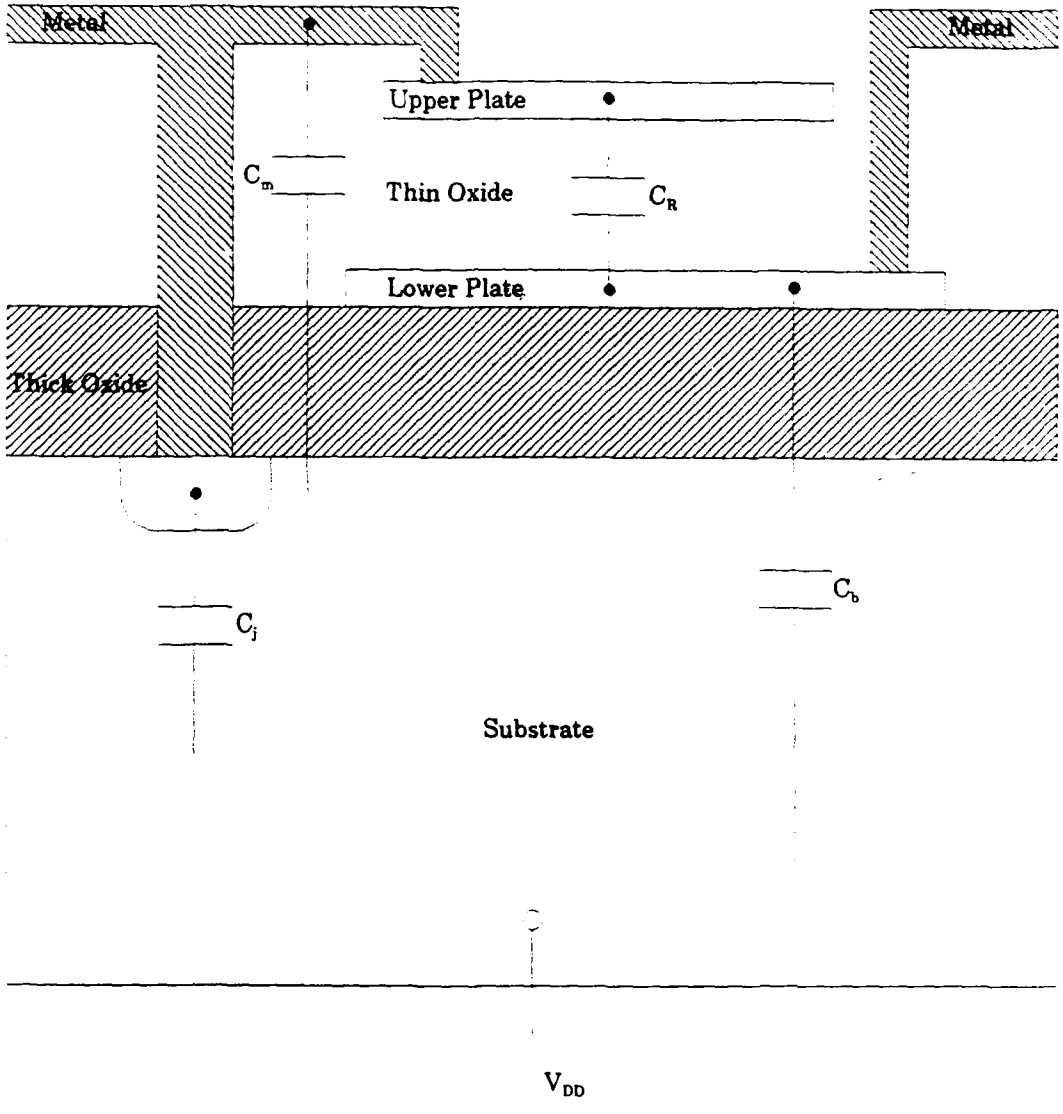

Figure 5.1 Silicon Realization of a MOS Capacitor

There are three parasitic capacitances shown in Figure 5.1.

1. Bottom Plate Parasitic Capacitance, C_b.
2. Metal Routing Parasitic Capacitance, C_m.
3. Voltage Dependent Nonlinear Parasitic Capacitance, C_j.

Bottom plate parasitic capacitance, C_b , is the parasitic capacitance that exists between the bottom plate and the substrate. Metal routing parasitic capacitance, C_m , is the accumulated parasitic capacitance formed by all the metal routing which connects the top plate to the various components. Voltage dependent nonlinear parasitic capacitance, C_j, is associated with the source-drain diffusions of the switches. The effects of metal routing parasitic capacitance and of voltage dependent nonlinear parasitic capacitance are normally lumped together into a single parasitic capacitance called top plate parasitic capacitance.

Bottom plate parasitic capacitance, C_b , has typical values between 10 and 20 percent of the total design value of the capacitor itself, C_R. Top plate parasitic capacitance, C_t (where $C_t = C_m + C_j$), has typical values between 1 and 5 percent of the total design value of the capacitor itself, C_R .

One common method used to nullify the effects of bottom plate parasitic capacitance is to connect the bottom plate of C_R to ground, to an independent voltage source, or to an OA output. This connection will not help to produce a more accurate C_R but it will reduce the accumulated parasitic capacitances at the OA virtual ground.

Parasitic capacitances are also manifested into the MOS capacitor through the gate-to-source and the gate-to-drain capacitance from the gates that perform all of the switching in the network. This is also the path for clock feed through problem. Though the clocks used in switched capacitor networks are not a part of the signal itself, the switches that produce the two phase nonoverlapping clocks, Φ_o and Φ_e, use this gate-to-source and gate-to-drain paths to introduce clock feed through into the circuit which causes signal contamination.

C. NULLIFYING STRAY CAPACITANCE IN A LOSSLESS INTEGRATOR

A simple lossless integrator circuit is shown in Figure 5.2. Figure 5.3 shows the SC implementation of the lossless integrator. Figure 5.4 shows the possible parasitic capacitances in this circuit. After simplification and combination of these capacitors the effective parasitic capacitance, C_p can be clearly shown in Figure 5.5. The effective parasitic capacitance was found by switching the clock through its two phases while applying the following three rules for nullifying stray (parasitic) capacitance:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.
2. Capacitances between the output of an OA and ground are inconsequential.
3. Capacitances that are driven by a voltage source are inconsequential.

Figure 5.5 shows that not all of the parasitic capacitance has been removed. After using the above three rules to nullify parasitic capacitance some stray capacitance still remains. Even though the effects of most of the stray capacitance has been nullified, there still exists some stray capacitance in this lossless integrator circuit.

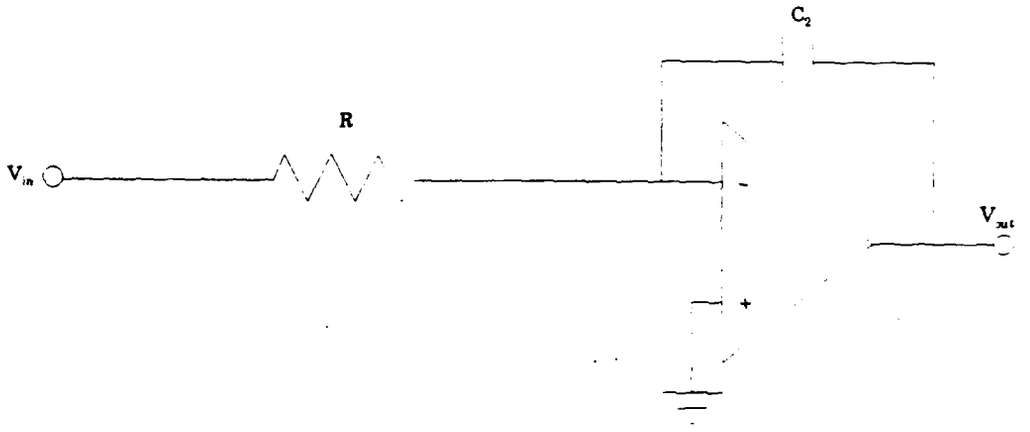

Figure 5.2 Lossless Integrator

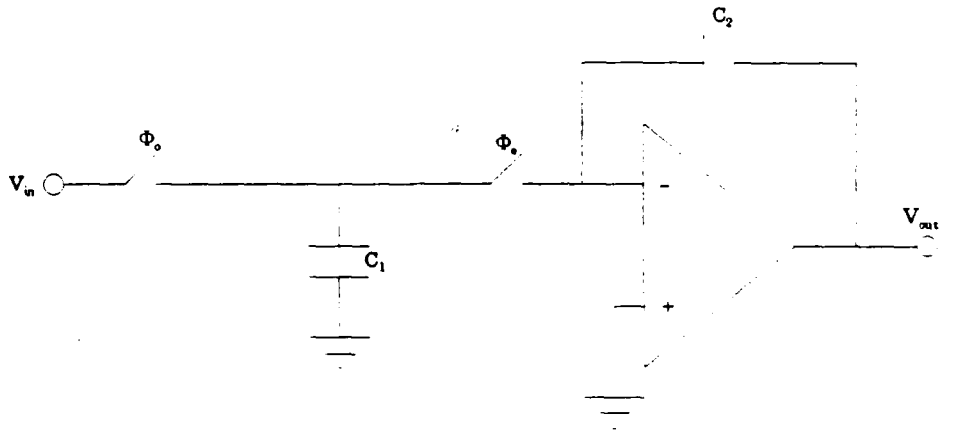

Figure 5.3 Switched Capacitor Implementation of the Lossless Integrator

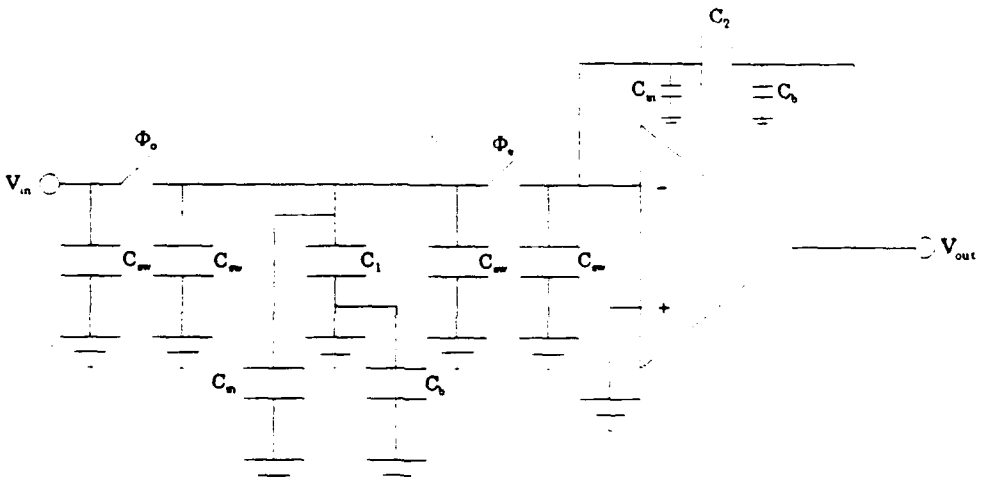

Figure 5.4 Switched Capacitor Lossless Integrator with Parasitic Capacitances

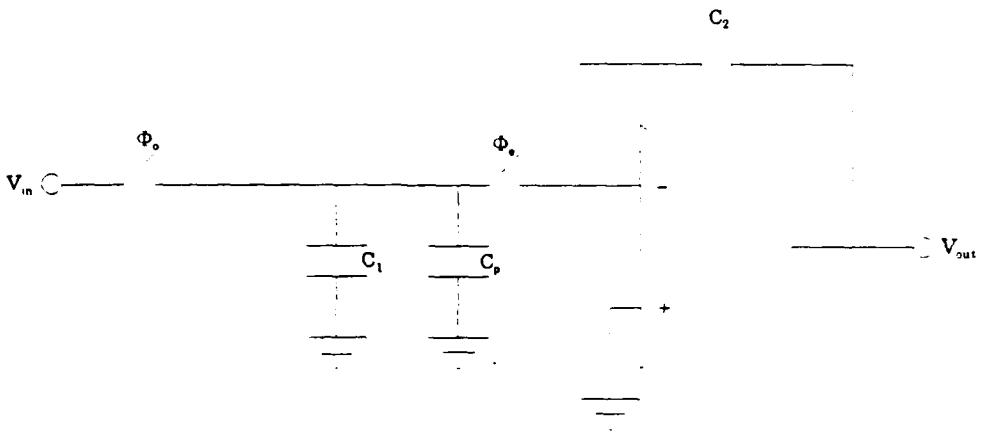

Figure 5.5 SC Lossless Integrator with Effective Parasitic Capacitance

The change in the transfer equation due to this effective parasitic capacitance can be quite detrimental. It can be easily shown that the transfer equation for the lossless integrator with parasitic capacitance is

$$\frac{V_{out}}{V_{in}} = \frac{\frac{C_1}{C_2}\left(1 + \frac{C_p}{C_1}\right) z^{-\frac{1}{2}}}{1 - z^{-1}} \tag{5.1}$$

The transfer equation for the lossless integrator without the effective parasite capacitance is

$$\frac{V_{out}}{V_{in}} = \frac{\frac{C_1}{C_2} z^{-\frac{1}{2}}}{1 - z^{-1}} \tag{5.2}$$

The error introduced by the effective parasitic capacitance is therefore

$$\frac{C_p}{C_2} \tag{5.3}$$

It may still be possible to reduce this error by ensuring that C_p is kept small or by ensuring that C_2 is kept sufficiently large. The value for C_p can be as high as 20% of the value of C_1 so keeping it small cannot be done. Any change in the value of C_2 changes the integrator circuit characteristics. Clearly there must be a better way to implement switched capacitor circuitry. The circuit topology can be altered in order to nullify the effects of this lasting parasitic capacitance. Many such circuit topologies exist, this thesis will focus on two, the toggle switched capacitor (TSC) and the modified open-circuit floating resistor (mOFR).

D. A STRAY INSENSITIVE SWITCHED CAPACITOR NETWORK

In order to eliminate the effect of the remaining parasitic capacitance, the TSC and the mOFR topologies combined with the seven guidelines listed below will be utilized.

1. Switched Capacitor Network Design and Layout Precautions

The following seven design and layout precautions for switched capacitor networks were found on pages 562 through 564 in Reference 11:

1. OAs must not be operated in open-loop fashion at any time, in order to avoid nonlinearities and saturation. A switched capacitor alone should not be used in the feedback loop. At a minimum add an unswitched capacitor to the feedback loop.

2. No circuit nodes must be completely isolated by capacitors. A path must exist either directly or through a switched capacitor to a voltage source to ground so that stray charge accumulations can be discharged. This implies that a the feedback path around an OA must be closed by a switched capacitor (dc feedback) in order to avoid charge accumulation at the summing node leading to saturation of the OA.

3. As explained earlier, the bottom plate of every capacitor should be connected either directly or through a switch to ground or to a voltage source.

4. The noninverting OA input should be kept at ac ground. If this input terminal is connected to a signal voltage, the circuit tends to become sensitive to all parasitic capacitors from switches, signal lines, and the substrate.

5. Provide separate bias lines for the analog and digital circuitry in the switched capacitor circuit. This will help prevent the switching noise from infiltrating the SC circuit.

6. Lines with digital signals should be kept as far away as possible from lines that carry the analog signal.

7. Due to sampling, clock feed through usually aliases down to dc and adds to the dc offsets of the OAs. Its origin is found in the gate-to-source or the gate-to-drain overlap capacitors of the switches at the inputs to the OAs. This effect can be minimized by maximizing the size of the unswitched feedback capacitor.

2. A Stray Insensitive TSC Implementation of the Lossy Integrator

Using both the seven switched capacitor network design and layout precautions and the three rules for nullifying stray capacitance, coupled with the toggle switched capacitor topology, the lossy integrator circuit will be transformed into a stray insensitive switched capacitor network. This transformation is performed pictorially in Figures 5.6 through 5.15.

The transfer equation for Figure 5.15 is

$$\frac{V_{out}}{V_{in}} = \frac{\frac{C_1}{C_2} z^{-\frac{1}{2}}}{1 - z^{-1}} \tag{5.4}$$

This equation clearly shows as does Figure 5.15 that a stray insensitive toggle switched capacitor lossy integrator can be made. The toggle switched capacitor (TSC) topology is one approach used to overcome the effective parasitic capacitance problem, another is the modified open-circuit floating resistor (mOFR) topology.

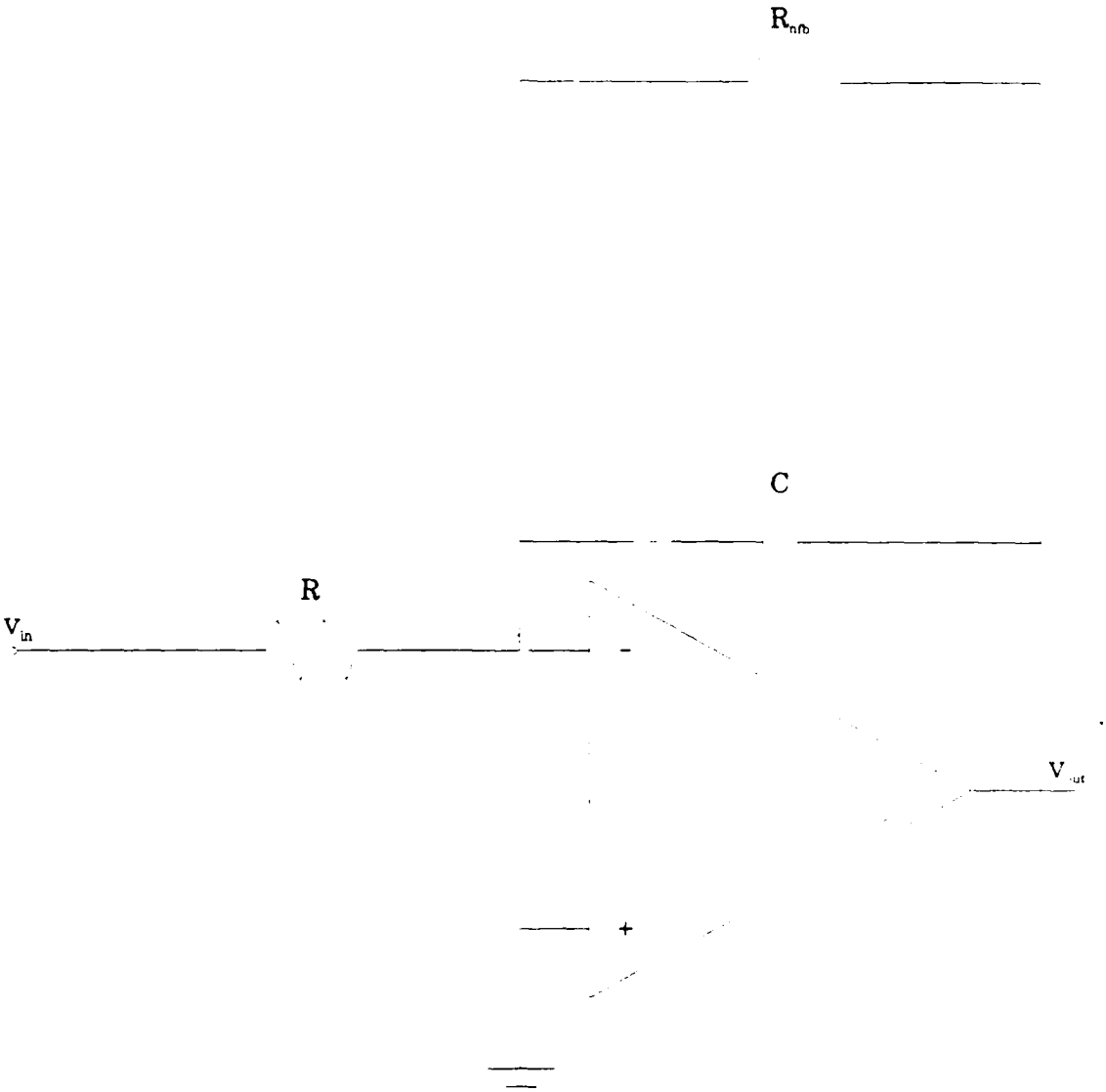

Figure 5.6 Lossy Integrator

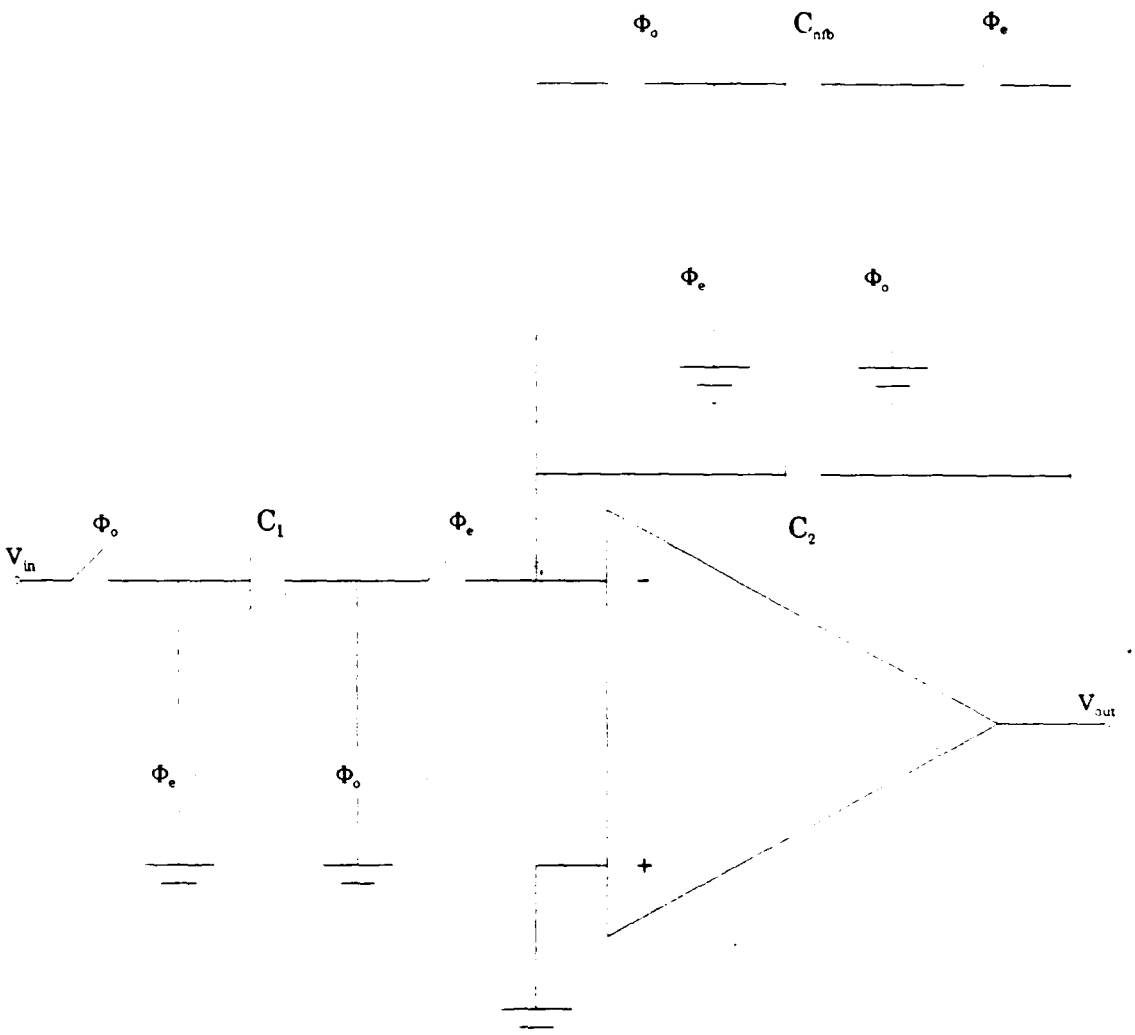

Figure 5.7 Toggle Switched Capacitor Implementation of the Lossy Integrator

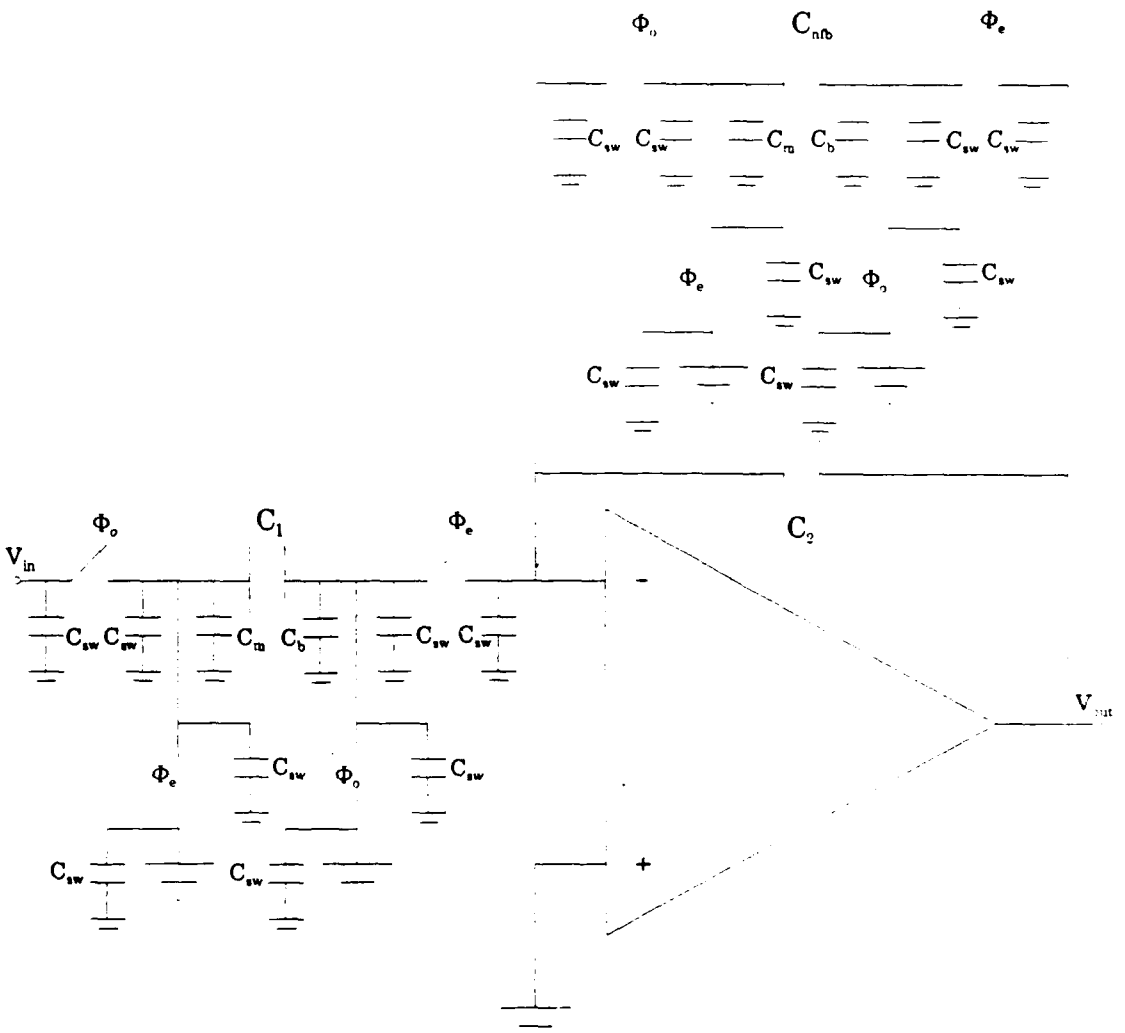

Figure 5.8 TSC Lossy Integrator with Stray Capacitances

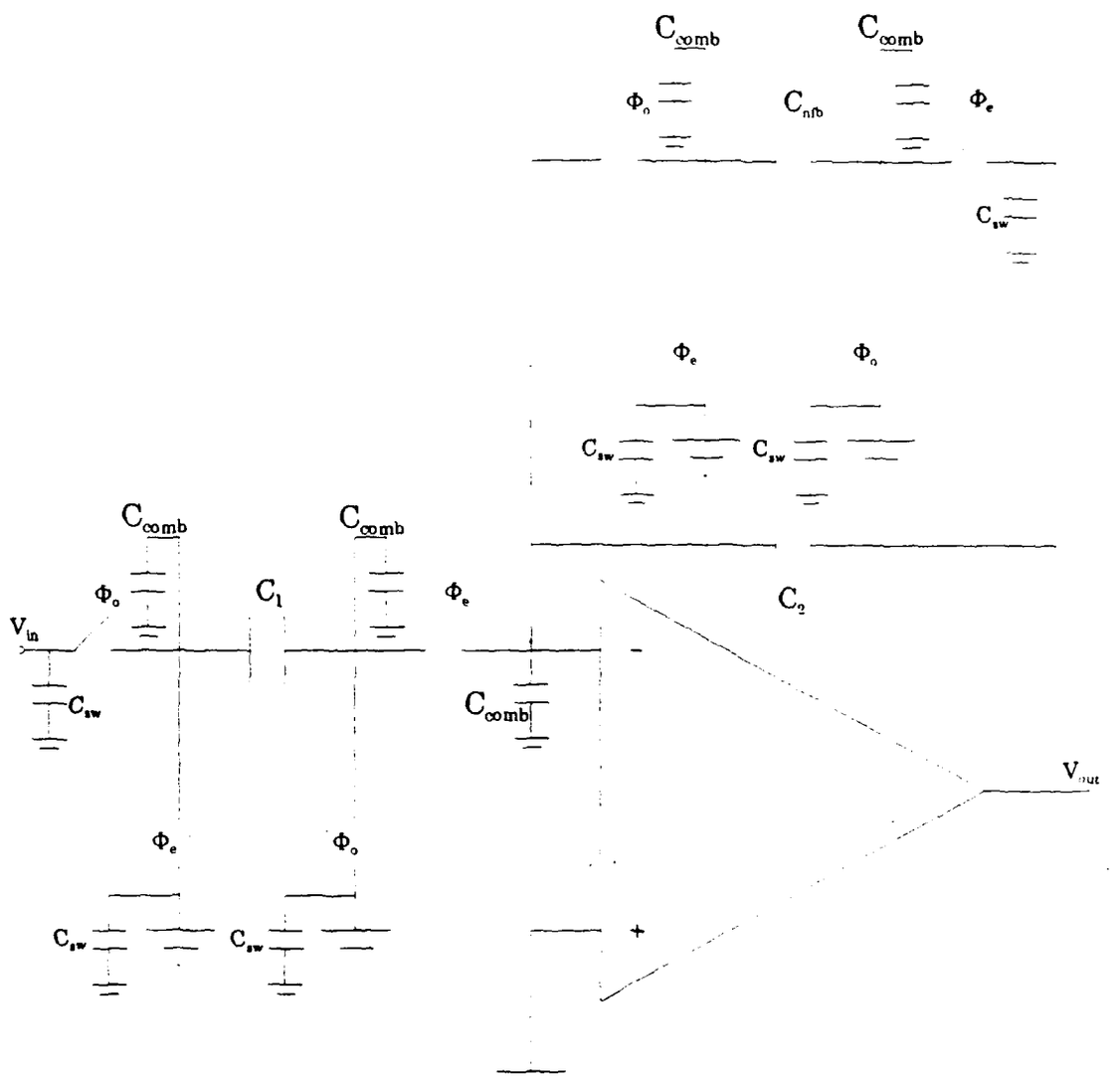

Figure 5.9 TSC Lossy Integrator with Combined Stray Capacitances

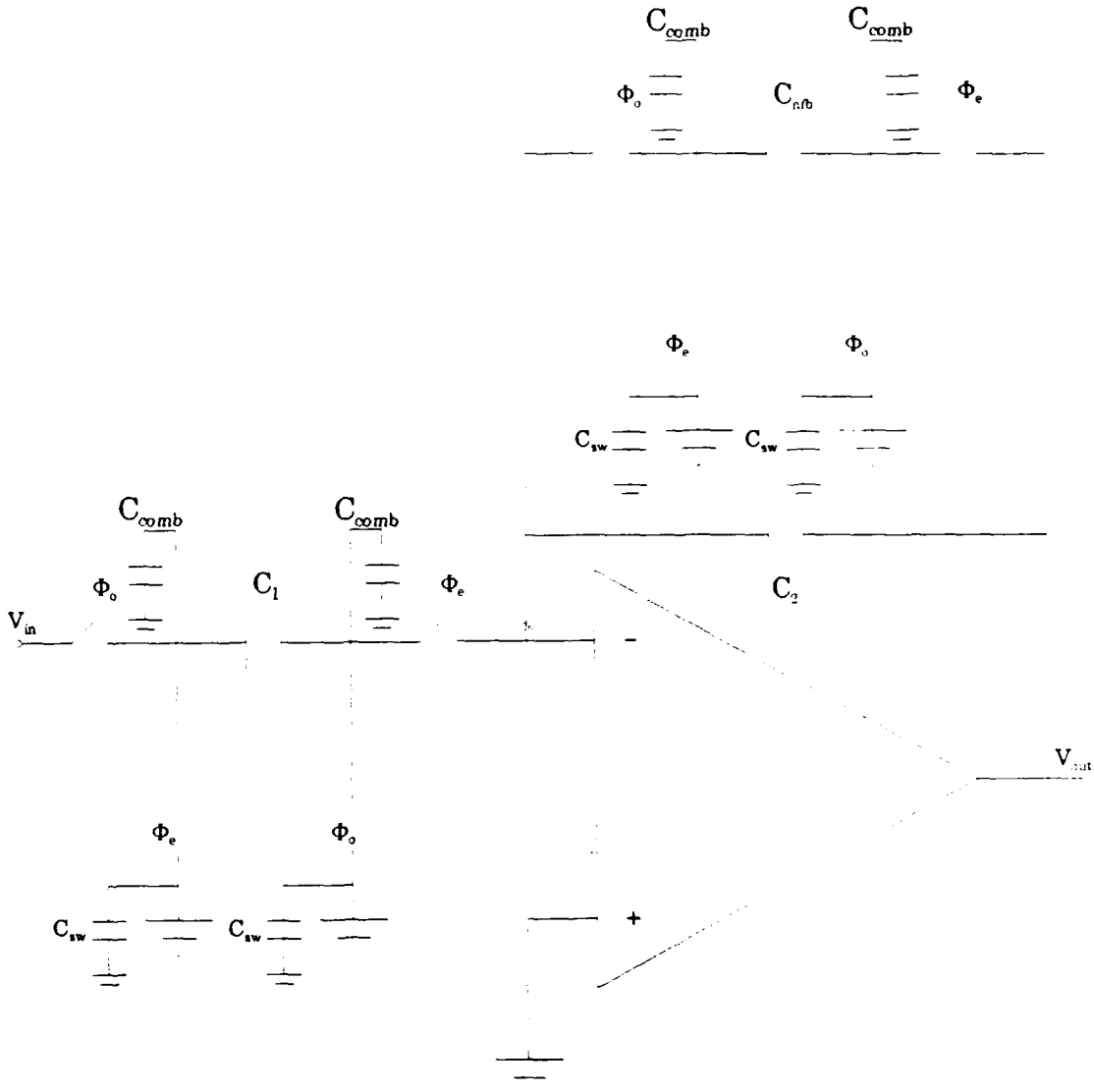

Figure 5.10 TSC Lossy Integrator with Reduced Combined Capacitances

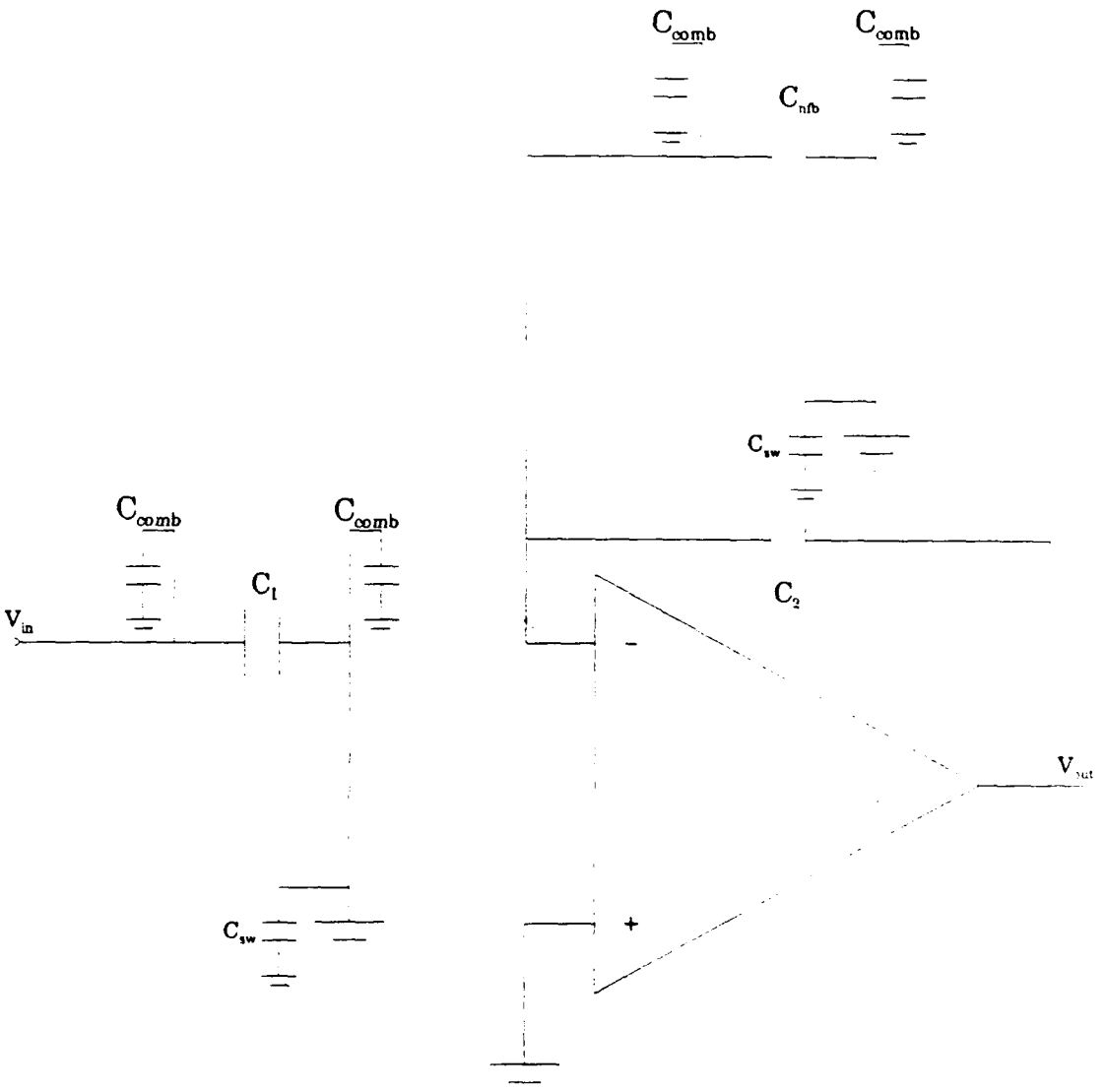

Figure 5.11 TSC Lossy Integrator with Odd Phase Clock Active

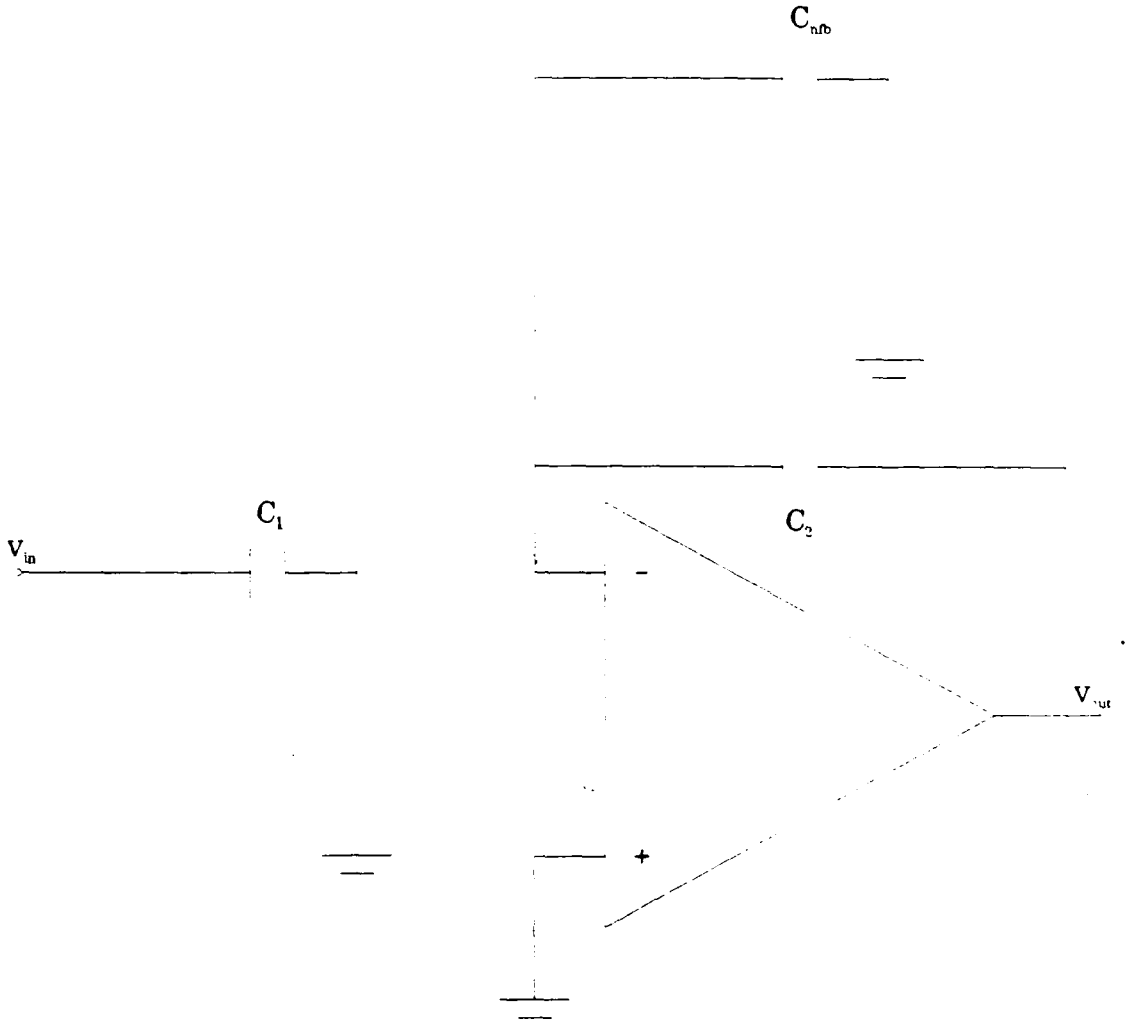

Figure 5.12 TSC Lossy Integrator with Φ_o Active and Effective Capacitances

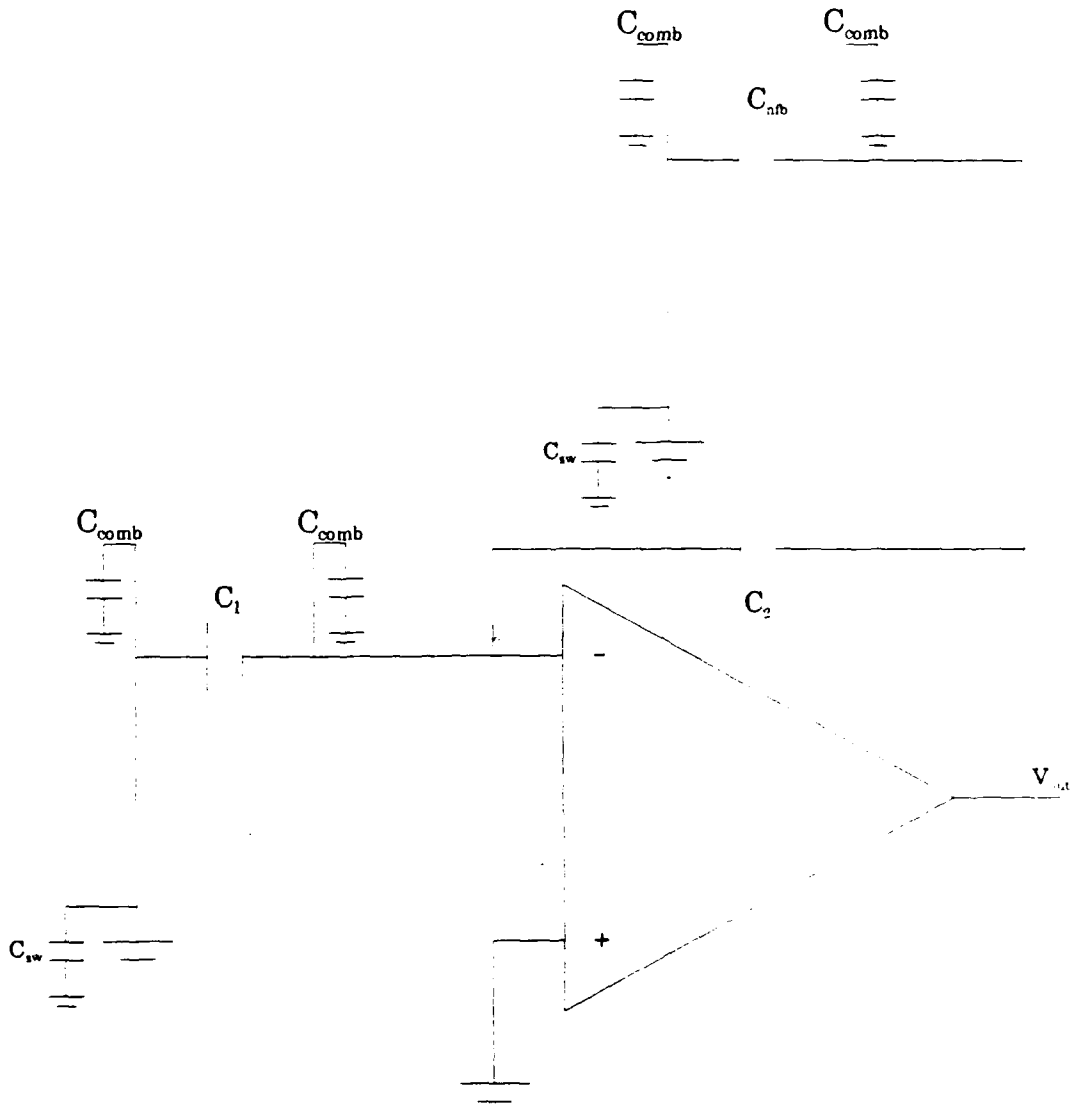

Figure 5.13 TSC Lossy Integrator with Even Phase Clock Active

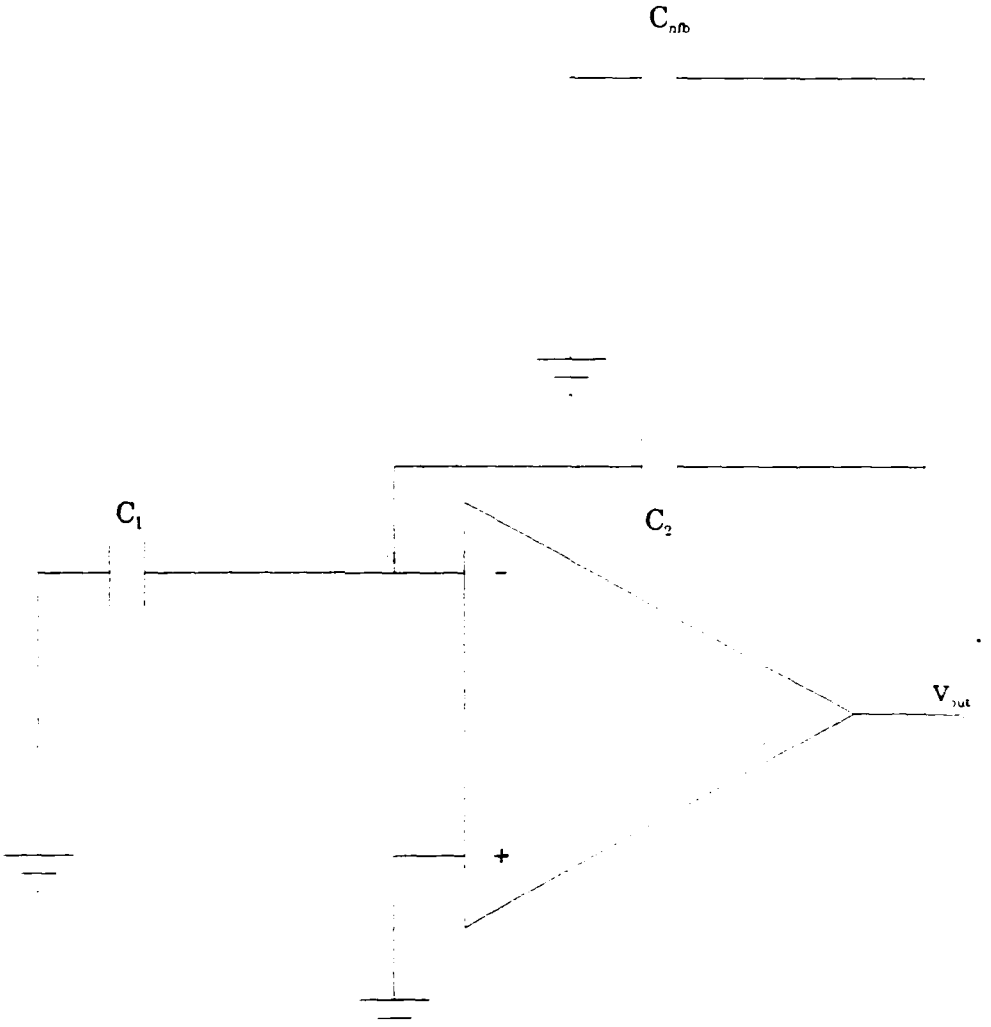

Figure 5.14 TSC Lossy Integrator with Φ_e Active and Effective Capacitances

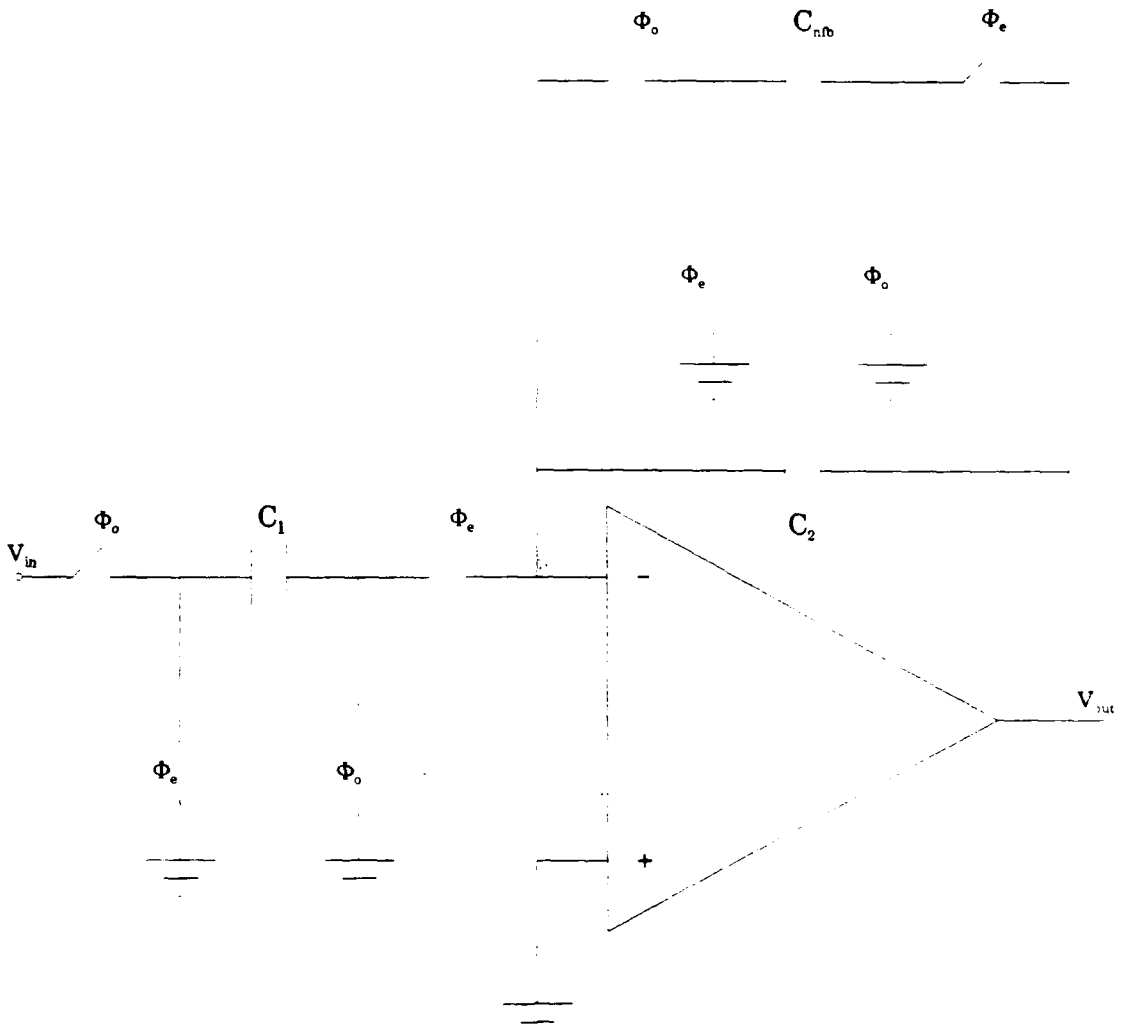

Figure 5.15 Stray Insensitive Toggle Switched Capacitor Lossy Integrator

3. A Stray Insensitive mOFR Implementation of the Lossy Integrator

Using both the seven switched capacitor network design and layout precautions and the three rules for nullifying stray capacitance, coupled with the modified open-circuit floating resistor topology, the lossy integrator circuit will be transformed into a stray insensitive switched capacitor network. This transformation is performed pictorially in Figures 5.16 through 5.25.

The transfer equation for Figure 5.25 is

$$\frac{V_{out}}{V_{in}} = \frac{\frac{C_1}{C_2} z^{-\frac{1}{2}}}{1 - z^{-1}} \tag{5.5}$$

This equation clearly shows as does Figure 5.25 that a stray insensitive modified open-circuit floating resistor lossy integrator can be made. The mOFR topology is the last approach that will be studied in this thesis to eliminate the effects of parasitic capacitance in switched capacitor networks.

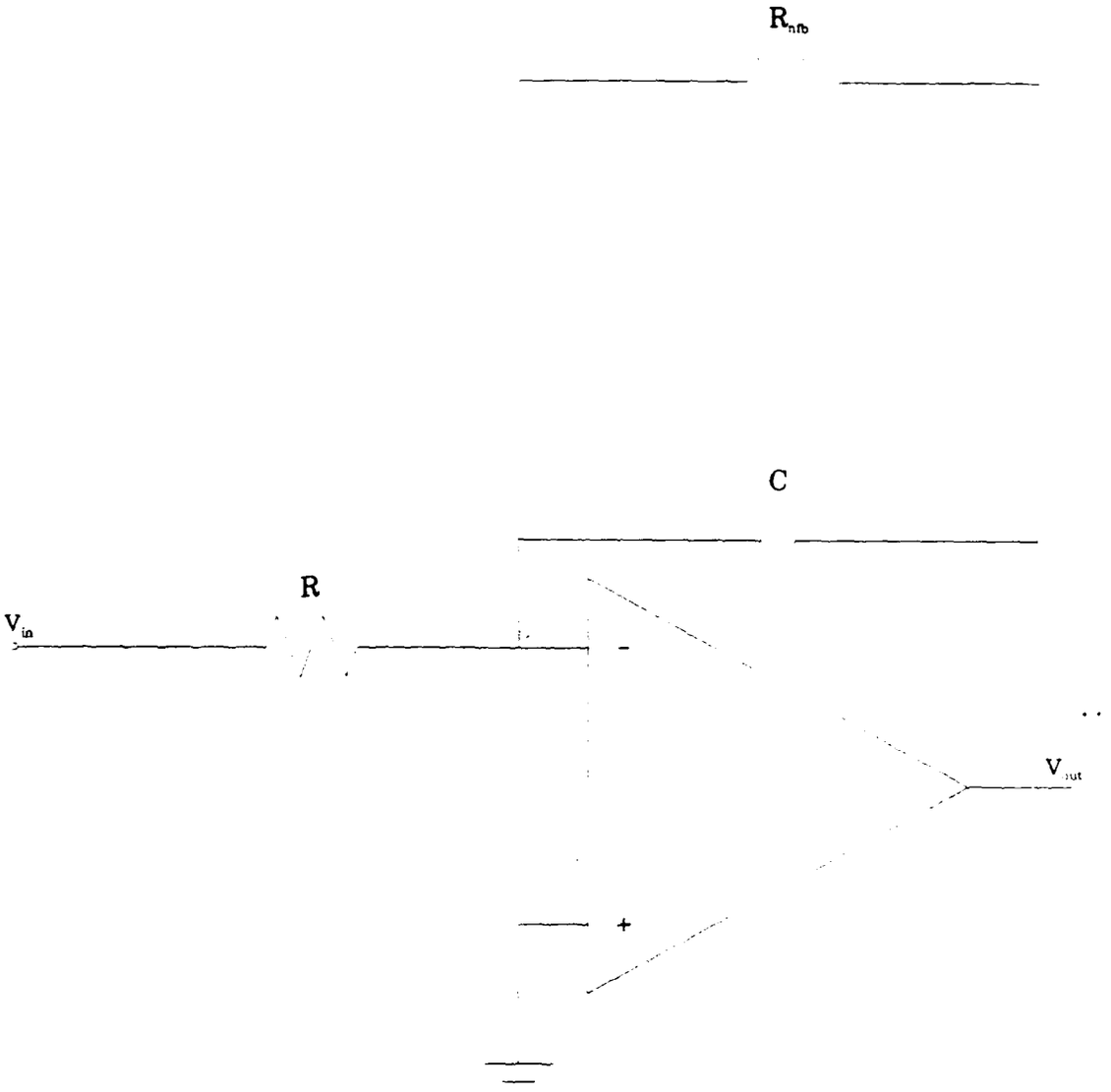

Figure 5.16 Lossy Integrator

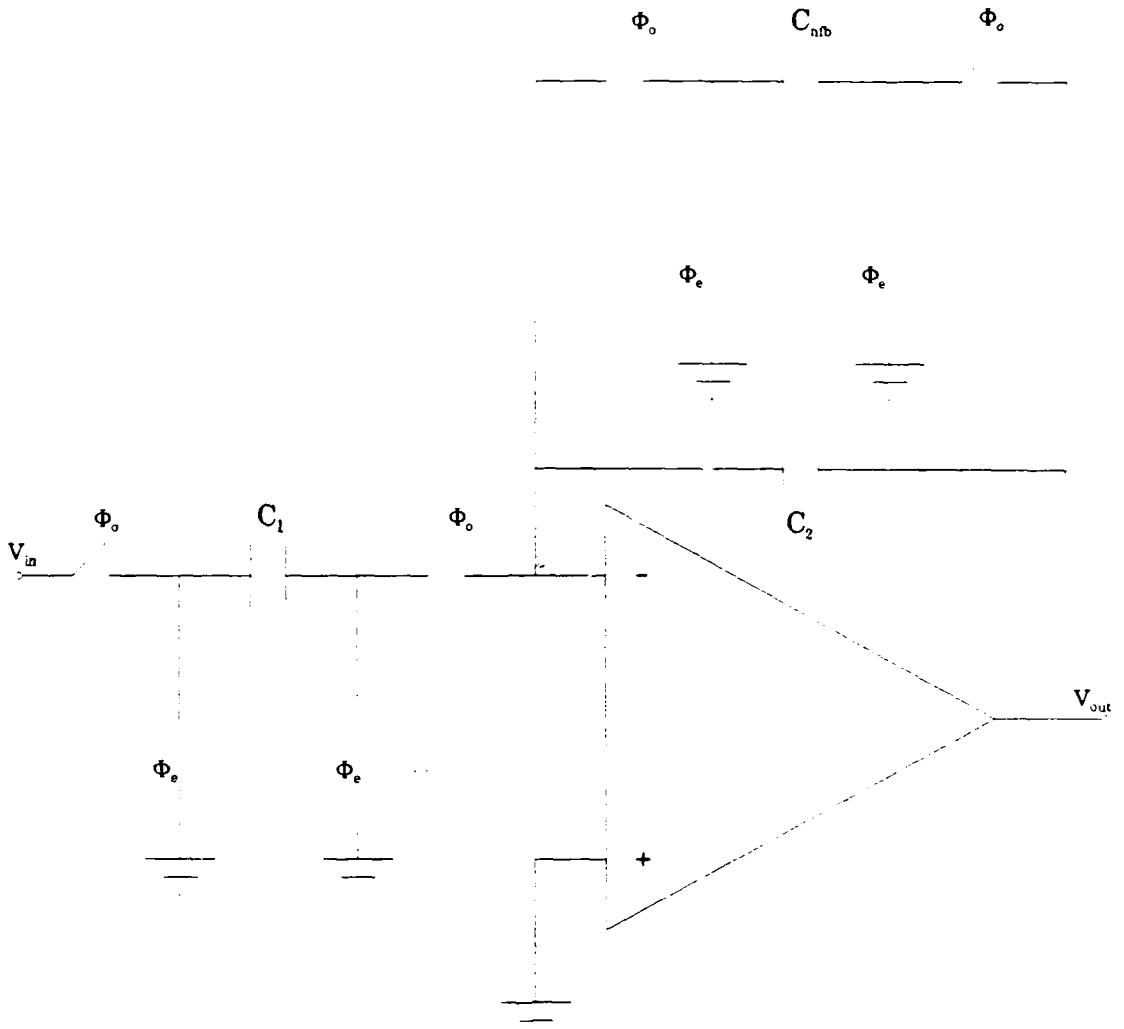

Figure 5.17 MOFR Implementation of the Lossy Integrator

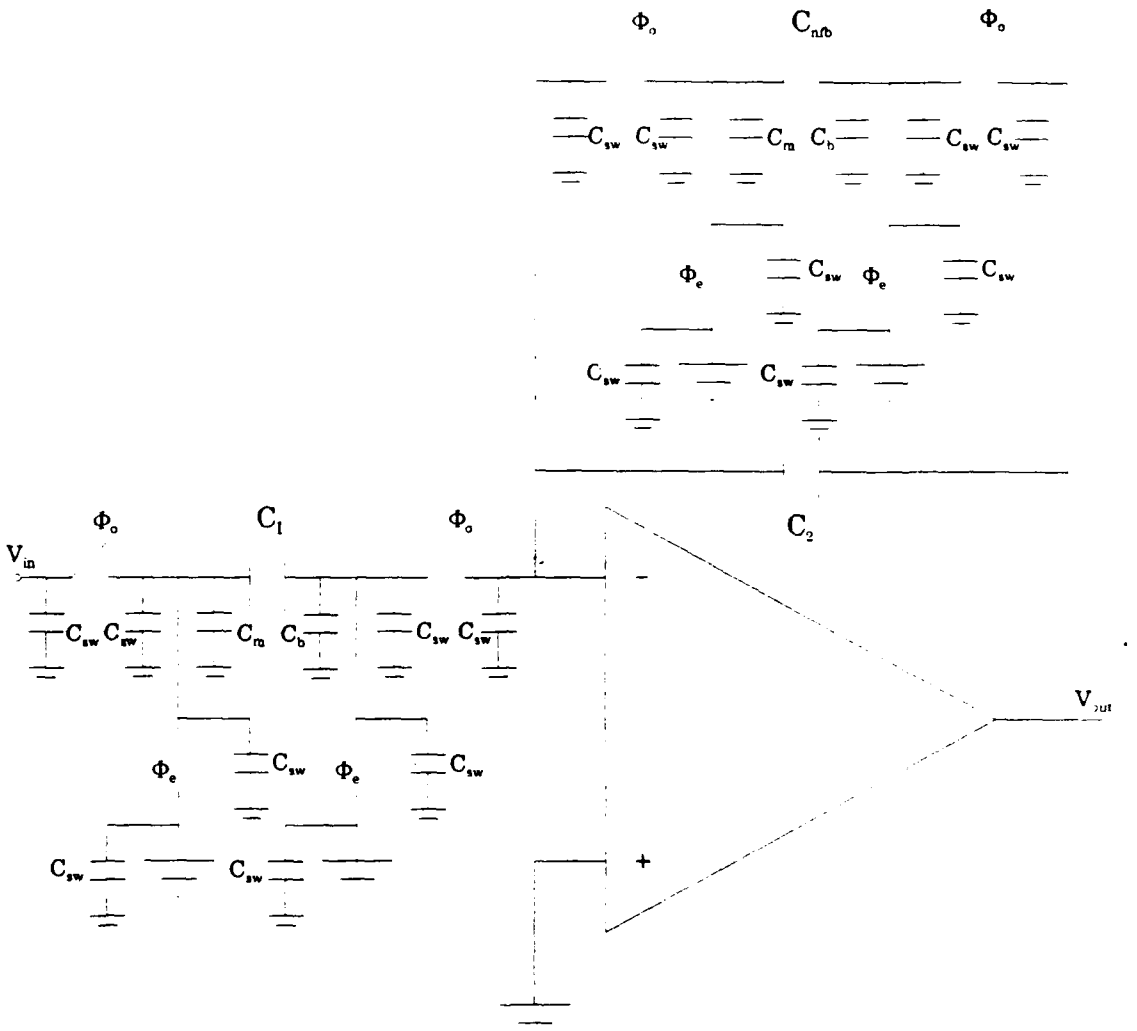

Figure 5.18 MOFR Lossy Integrator with Stray Capacitances

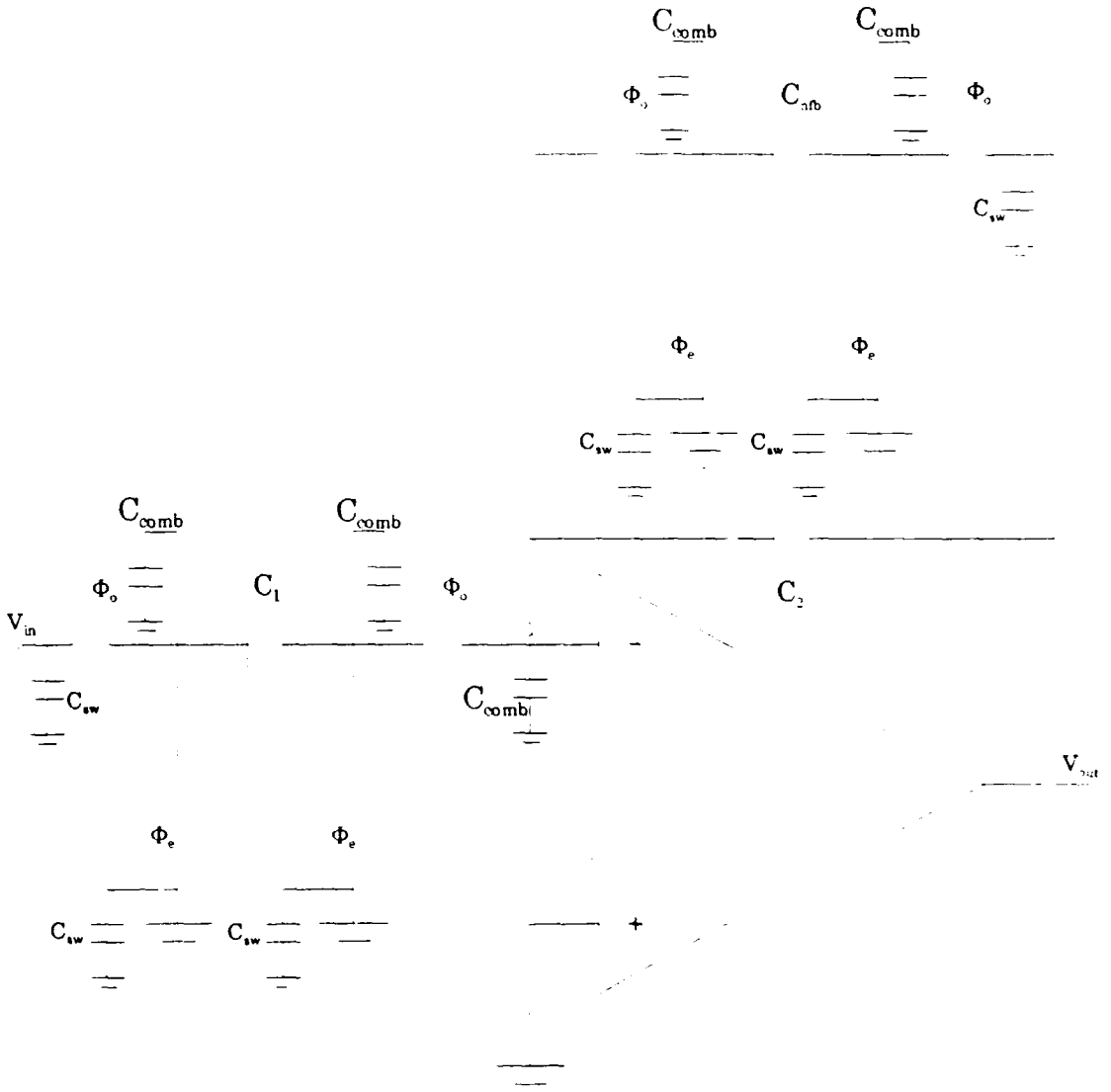

Figure 5.19 MOFR Lossy Integrator with Combined Stray Capacitances

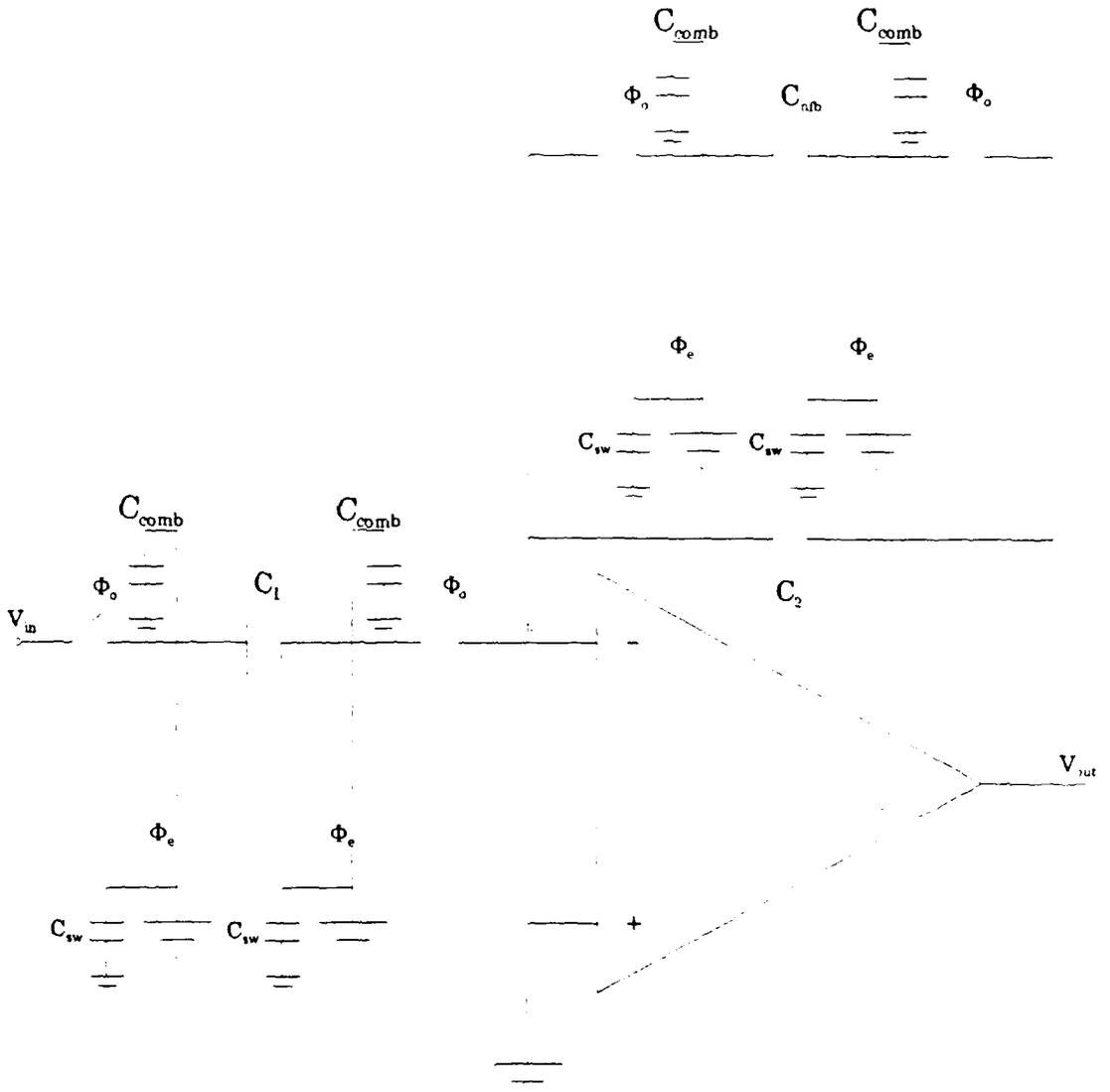

Figure 5.20 MOFR Lossy Integrator with Reduced Stray Capacitances

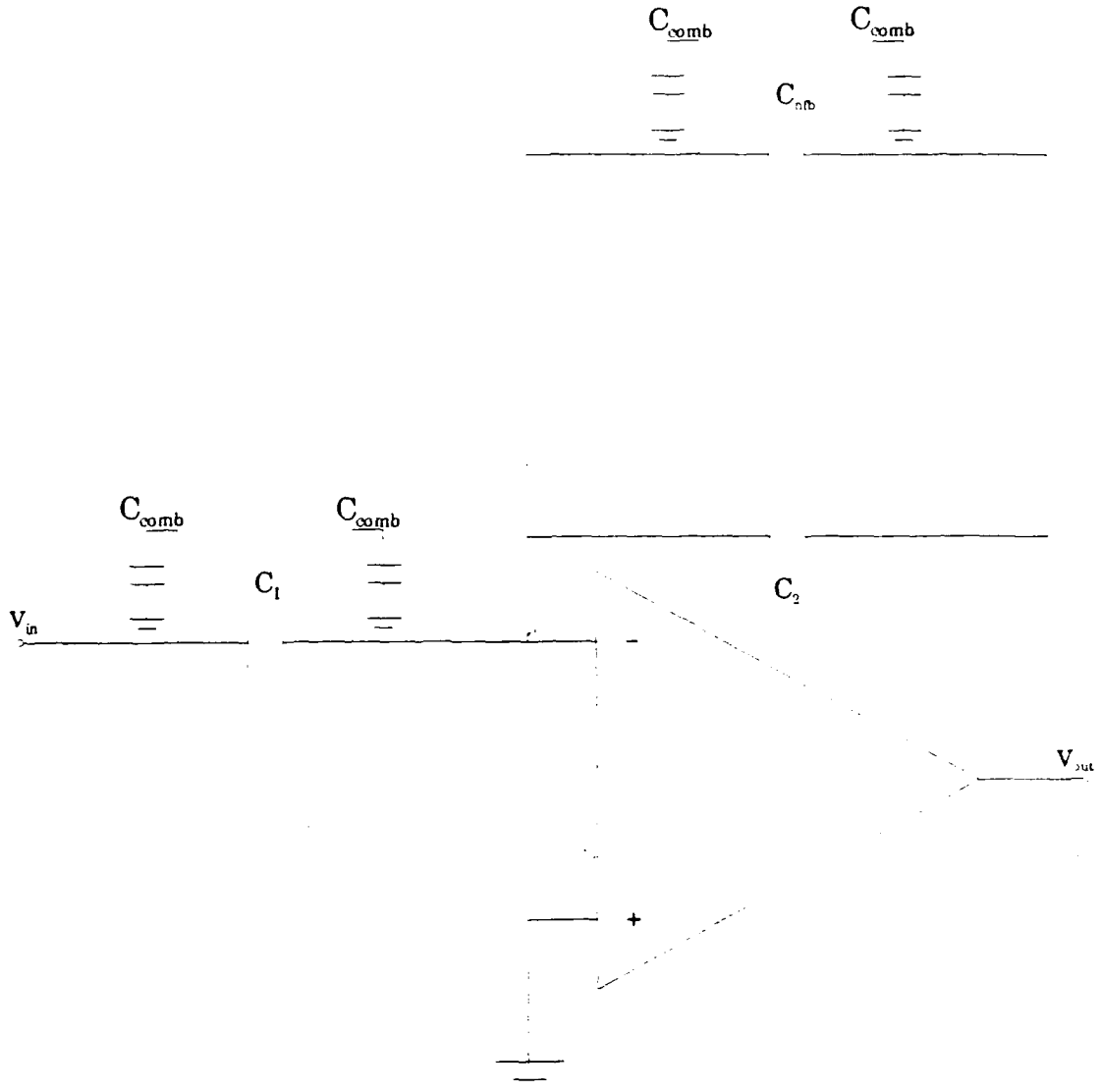

Figure 5.21 MOFR Lossy Integrator with Odd Phase Clock Active

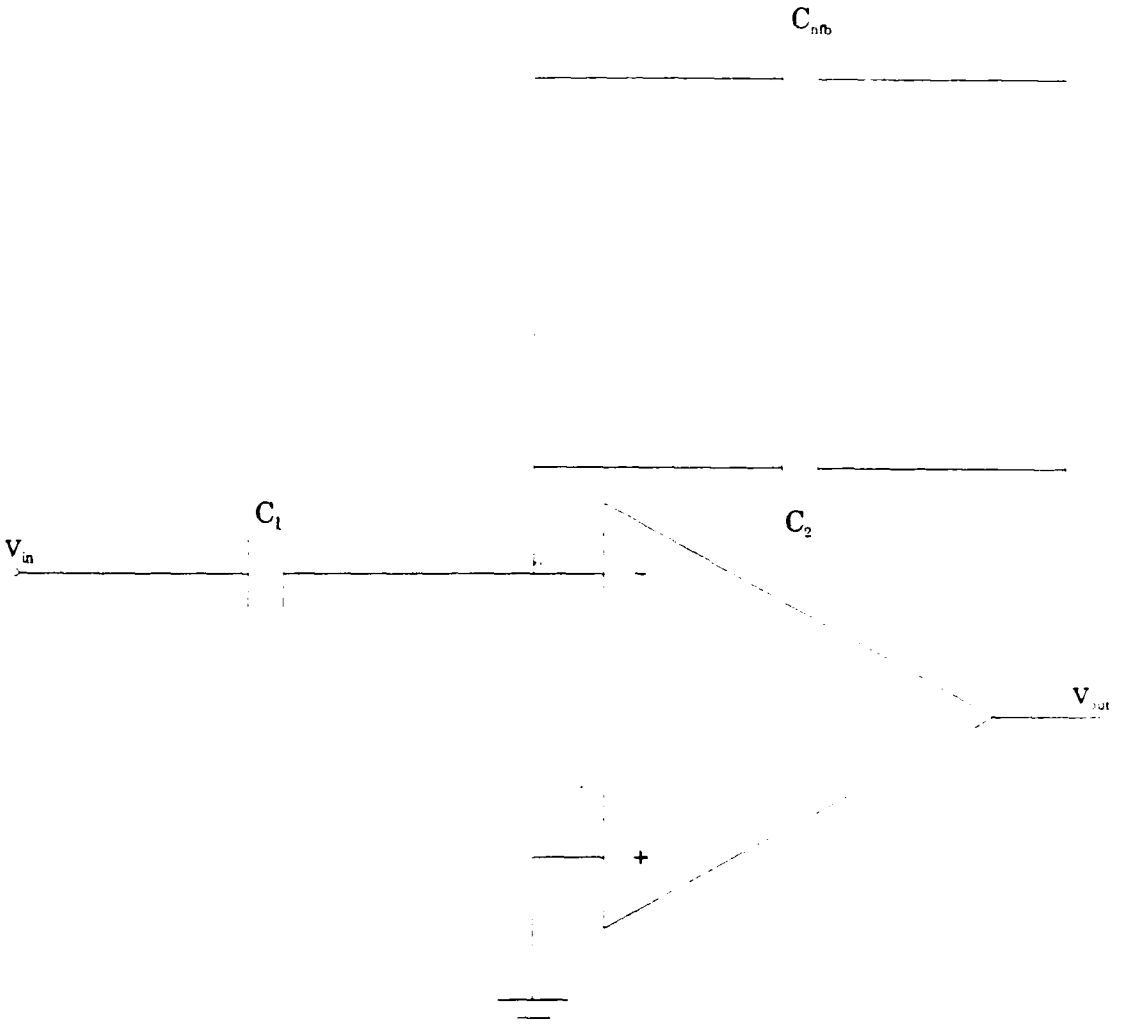

Figure 5.22 MOFR Lossy Integrator with Φ_o Active and Effective Capacitances

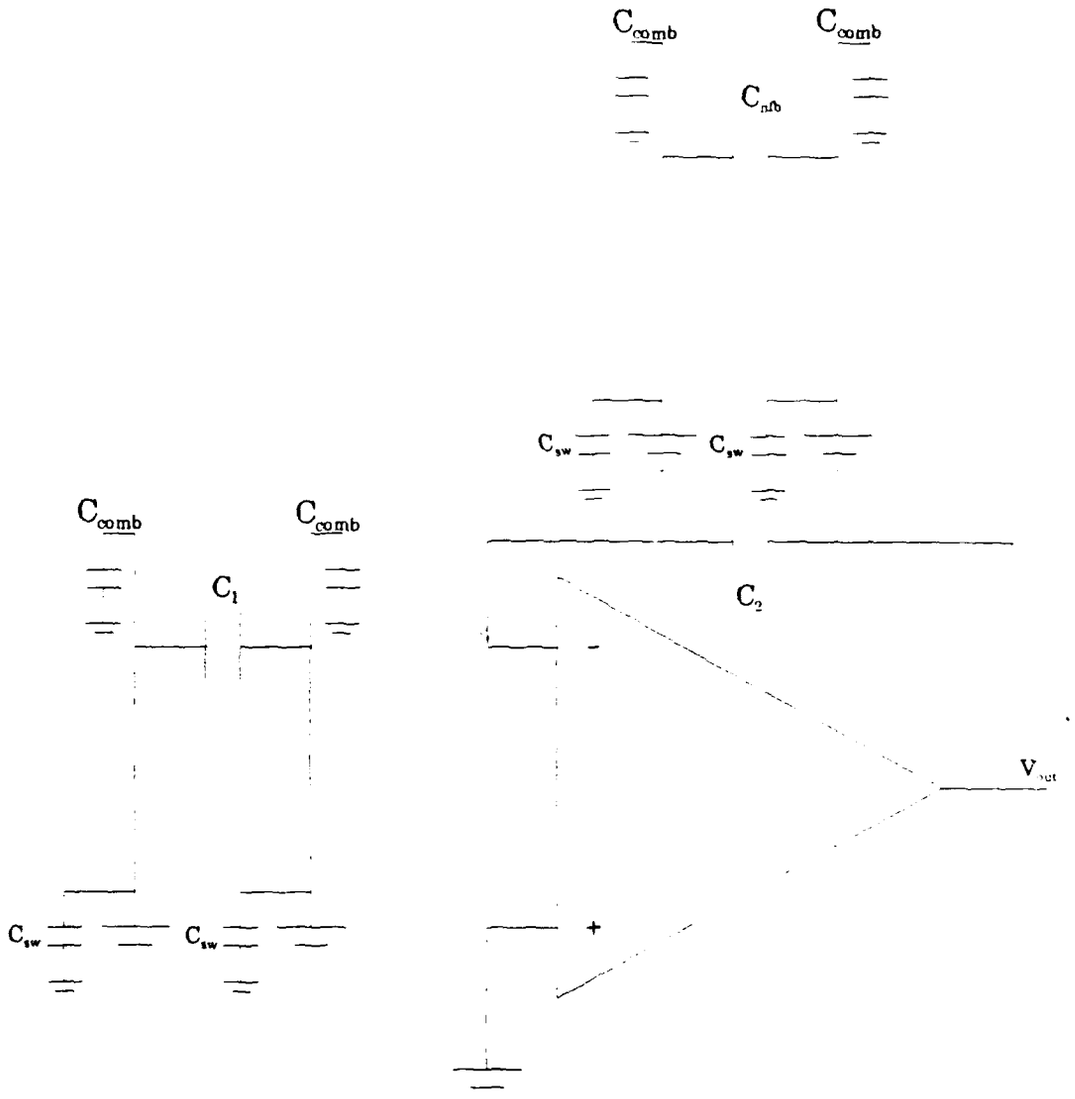

Figure 5.23 MOFR Lossy Integrator with Even Phase Clock Active

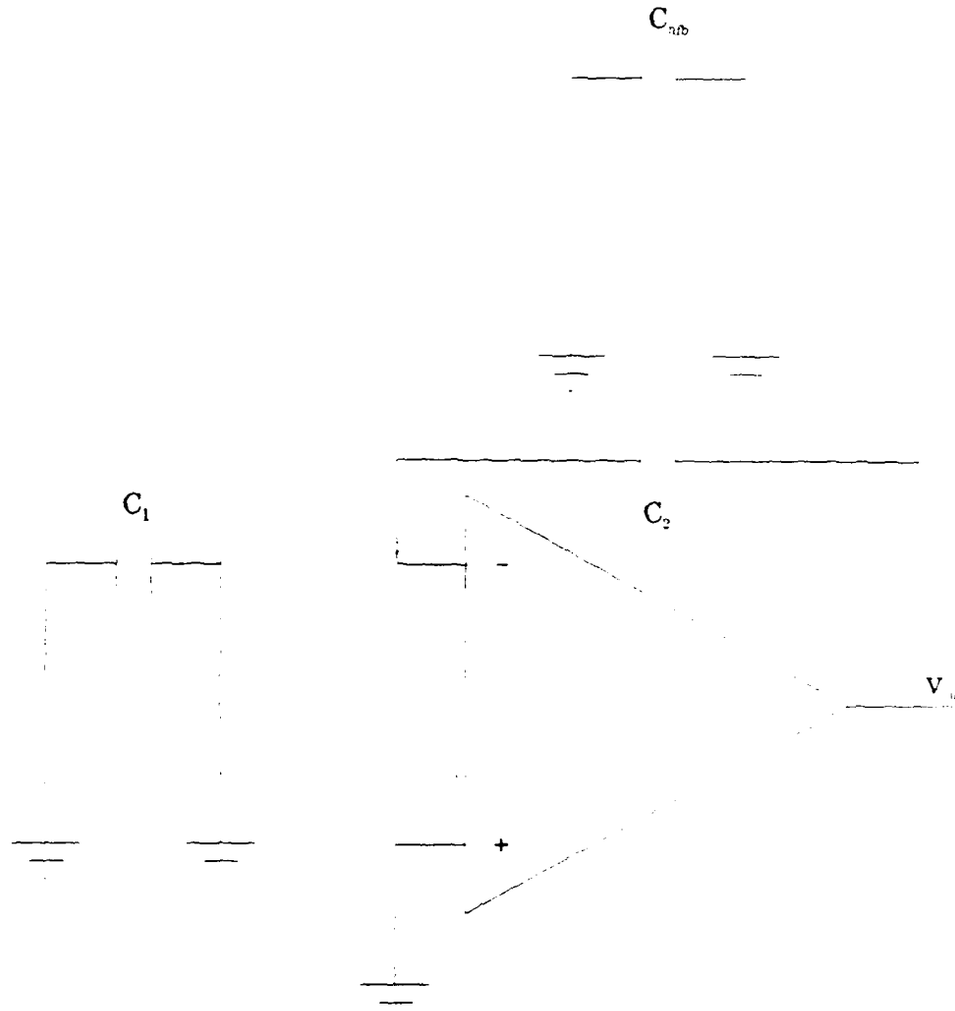

Figure 5.24 MOFR Lossy Integrator with Φ_e Active and Effective Capacitances

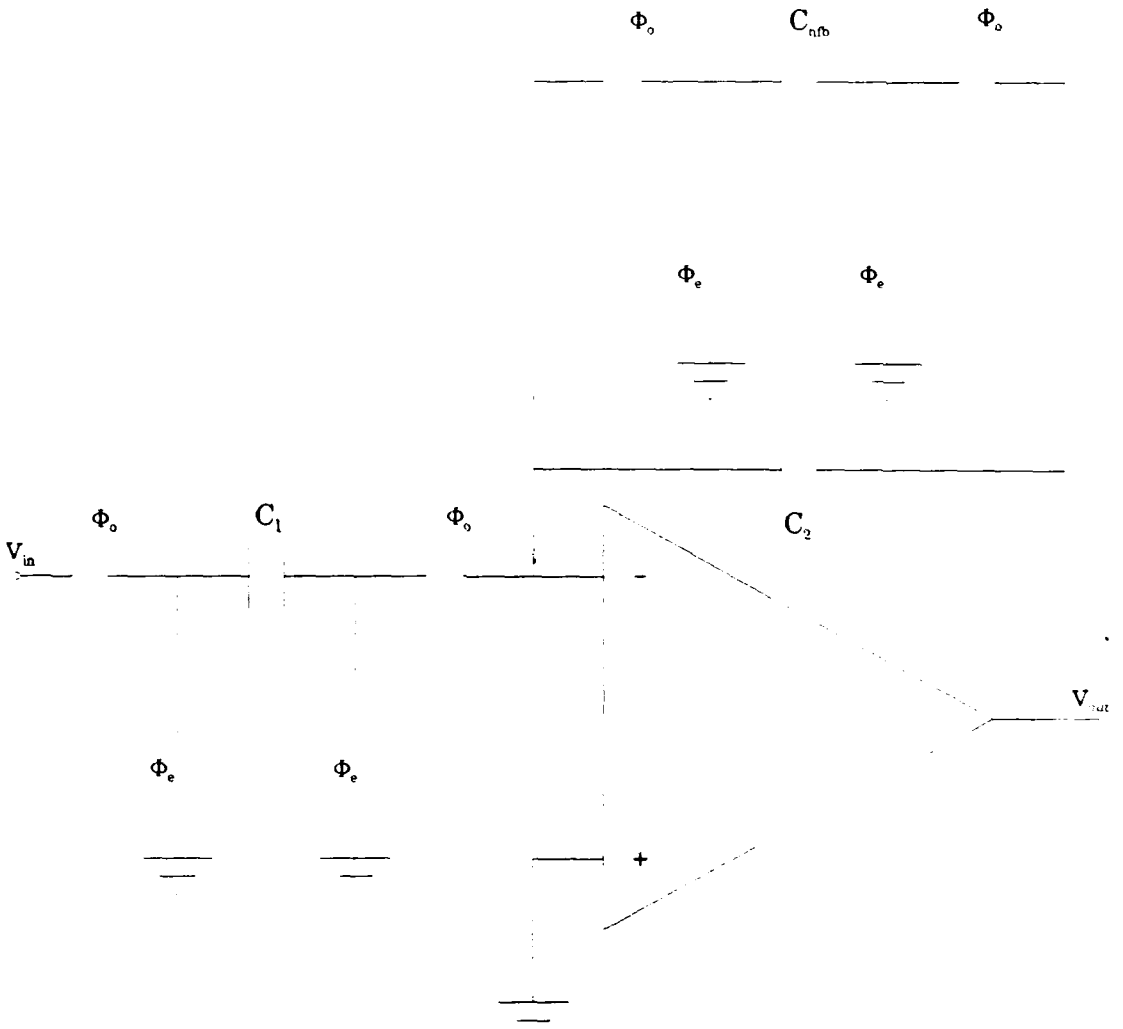

Figure 5.25 Stray Insensitive MOFR Lossy Integrator

E. SUMMARY

Stray insensitive switched capacitor networks can be easily designed and implemented using a total of ten guidelines and an effective circuit topology. The toggle switch capacitor and the modified open-circuit floating resistor are two such topologies. In the next chapter the four designs of the composite operational amplifiers that were introduced earlier in this thesis will be pictorially developed into stray insensitive networks.

VI. STRAY INSENSITIVE SWITCHED CAPACITOR COMPOSITE AMPLIFIERS

A. DESIGN OF THE STRAY INSENSITIVE C2OA-1 AND C2OA-2

The stray insensitive switched capacitor implementation of C2OA-1 and C2OA-2 will be developed pictorially in the next four sections. Each of the two composite OAs will be implemented in both the toggle switched capacitor (TSC) and the modified open-circuit floating resistor (mOFR) designs. These four designs will be pictorially displayed in ten separate figures with letters depicting each of the ten steps, therefore, similar lettered figures in each of the four designs will be at the same stage of development.

The four designs will be presented in the following order:

1. Toggle switched capacitor implementation of C2OA-1.
2. Toggle switched capacitor implementation of C2OA-2.
3. Modified open-circuit floating resistor implementation of C2OA-1.
4. Modified open-circuit floating resistor implementation of C2OA-2.

B. TOGGLE SWITCHED CAPACITOR C2OA-1

1. C2OA-1

Figure 6.1a on the next page depicts C2OA-1 in its original form as designed from nullator and norator modeling and having passed the four required performance criteria as set forth in Chapter III. The three-terminal equivalent is shown to the upper right.

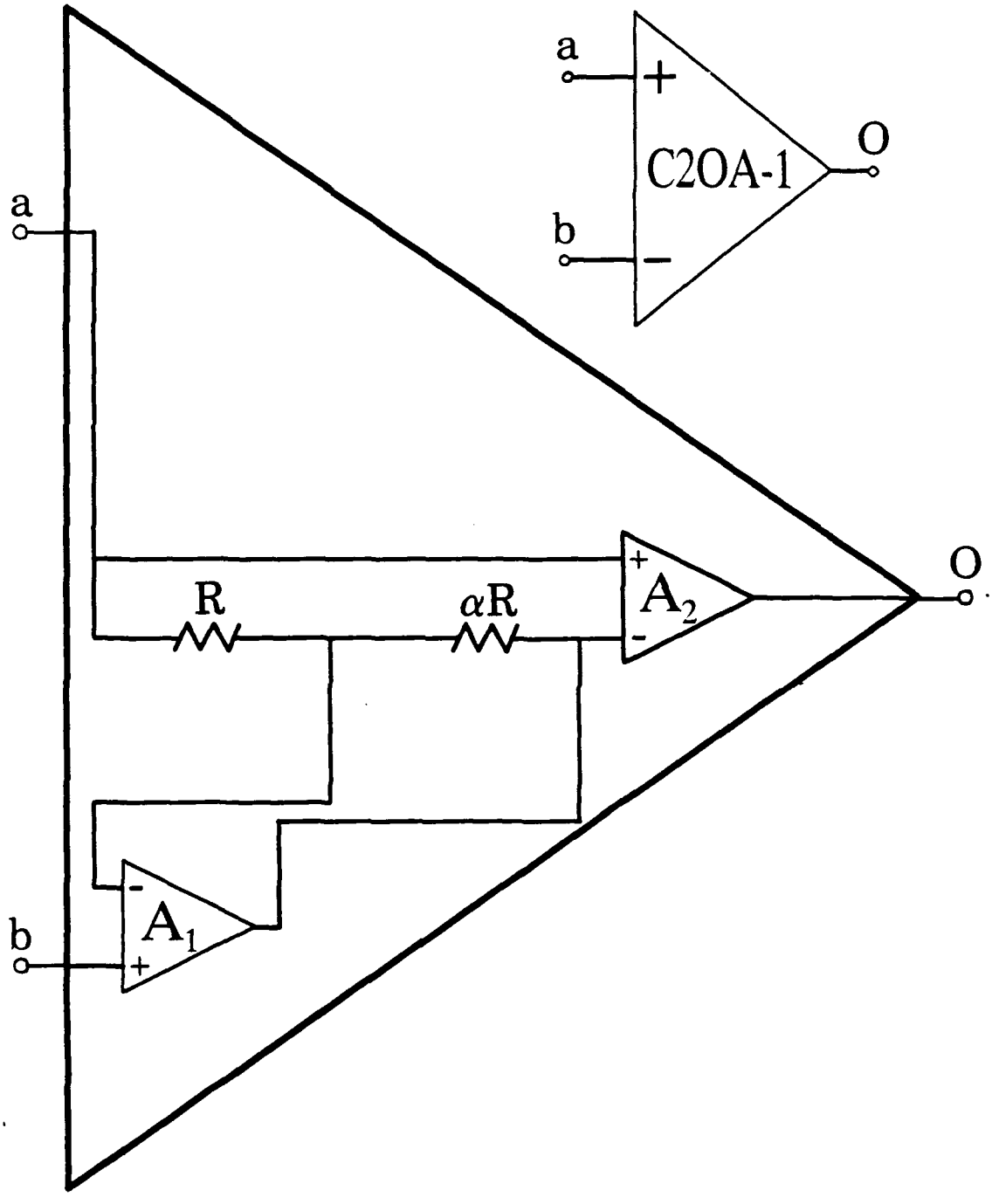

Figure 6.1a C2OA-1

2. TSC C2OA-1

Figure 6.1b realizes the toggle switched capacitor equivalent for the two resistors from the basic C2OA-1 form. Chapter IV detailed this transformation. In order to avoid nonlinearities and saturation, two capacitors, labeled C_{nfb} , were added.

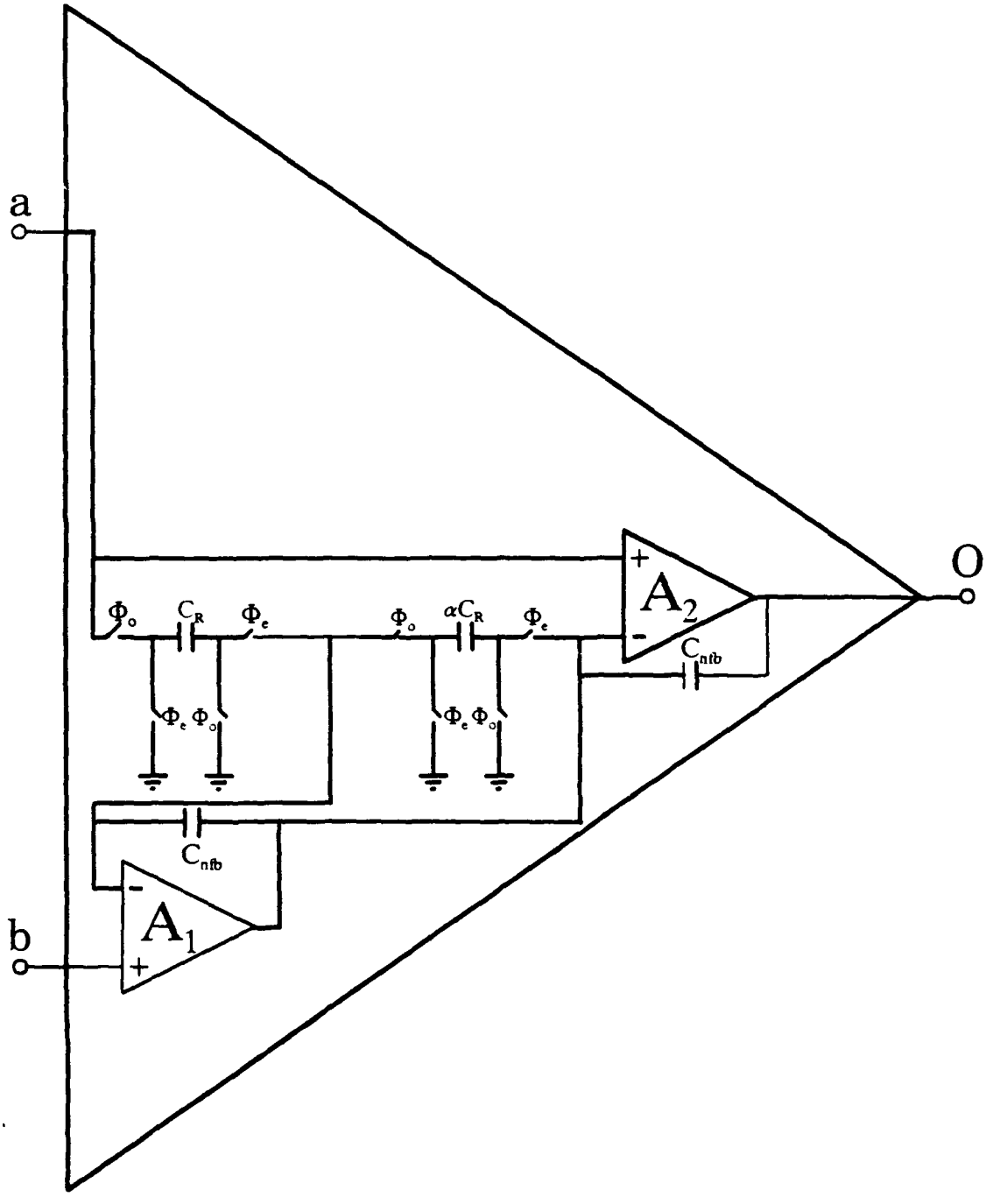

Figure 6.1b TSC C2OA-1

3. TSC C2OA-1 with Stray Capacitances

Figure 6.1c reflects the design with all possible stray capacitances added to the circuit as discussed in Chapter V. Not all of these stray capacitances actually exist, nor will all of them remain in the circuit if the design is well made. A good switched capacitor design will remove most, if not all, of the stray capacitances that were artificially introduced in the design.

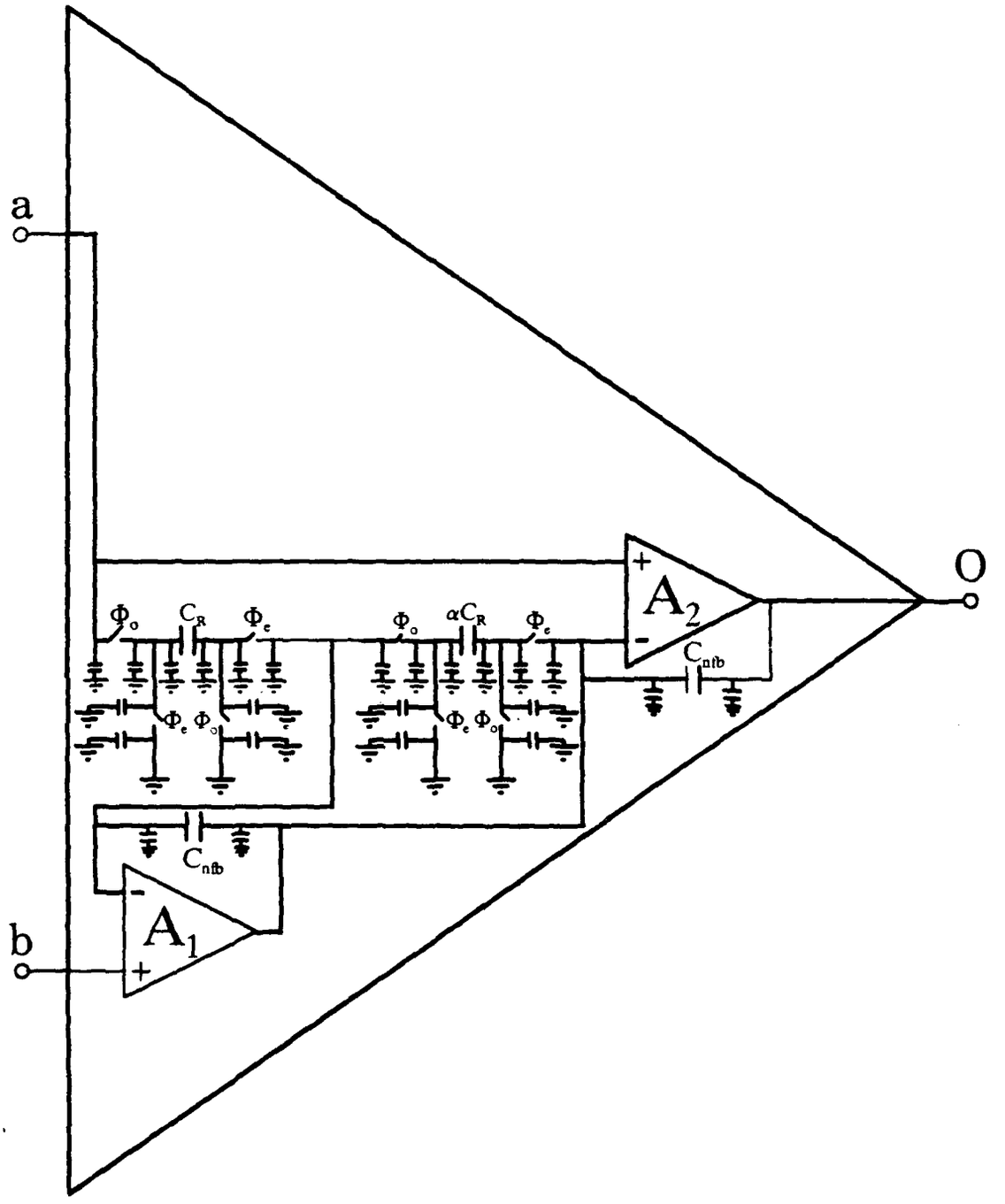

Figure 6.1c TSC C2OA-1 with Stray Capacitances

4. TSC C2OA-1 with Combined Stray Capacitances

Figure 6.1d combines the stray capacitances at each node into a single stray capacitance in order to simplify the circuit. The combined capacitors have been placed in the figure at a different position than any of the uncombined capacitors previously held so that they might present themselves more readily

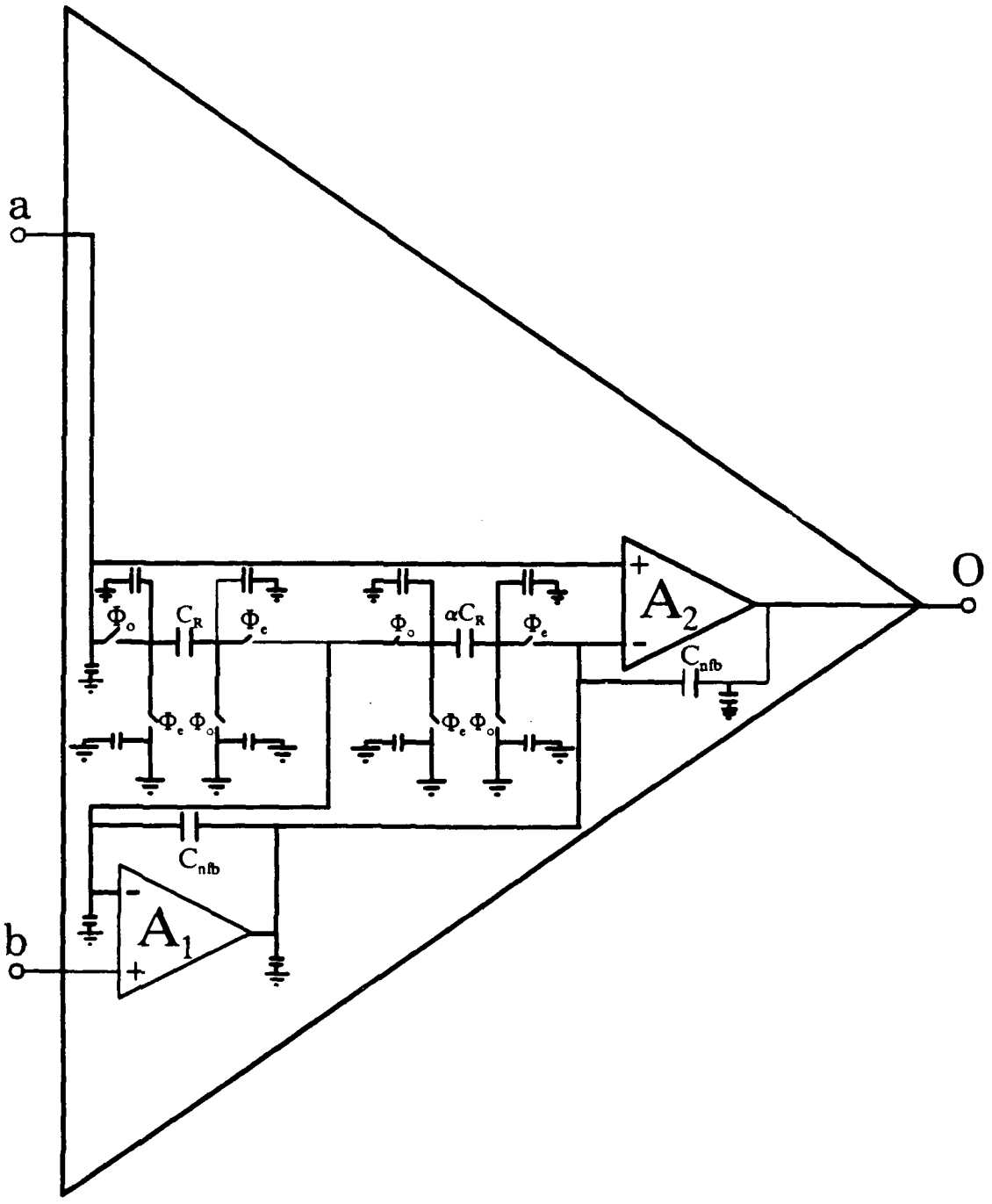

Figure 6.1d TSC C2OA-1 with Combined Stray Capacitances

5. TSC C2OA-1 with Reduced Stray Capacitances

Figure 6.1e removes some of the stray capacitances from the design. This reduction in stray capacitances was detailed in Chapter V and is summarized here below:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.
2. Capacitances between the output of an OA and ground are inconsequential.
3. Capacitances that are driven by a voltage source are inconsequential.

The remaining stray capacitances are not necessarily effective stray capacitances. The TSC topology must first be allowed to further reduce these parasitic capacitances.

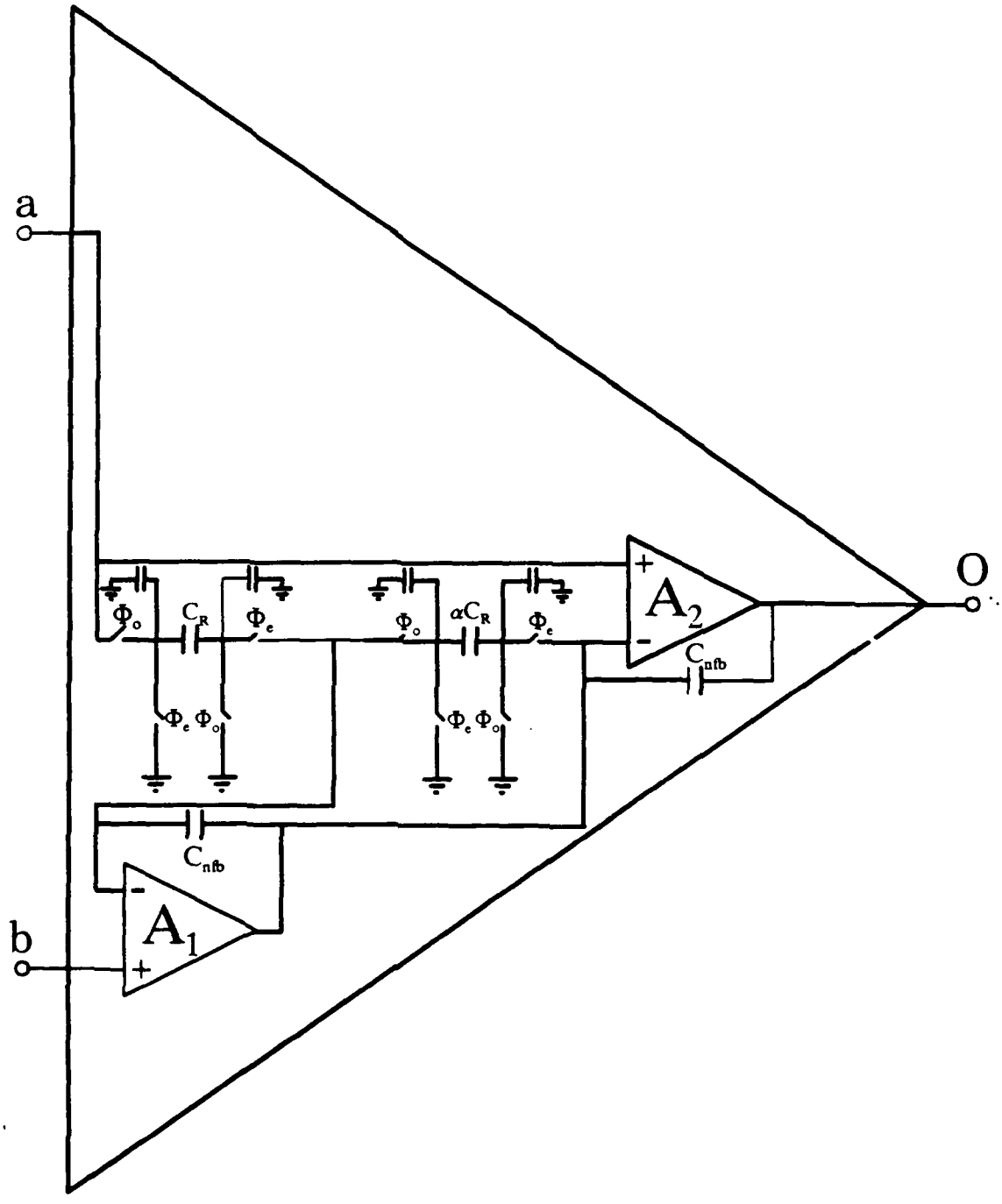

Figure 6.1e TSC C2OA-1 with Reduced Stray Capacitances

6. TSC C2OA-1 with Odd Phase Active

Figure 6.1f has the Φ_o clock active. This closes the four Φ_o switches and leaves the four Φ_e switches open and eliminates some of the circuit's complexity. The goal here is to ascertain which stray capacitances, if any, can be eliminated.

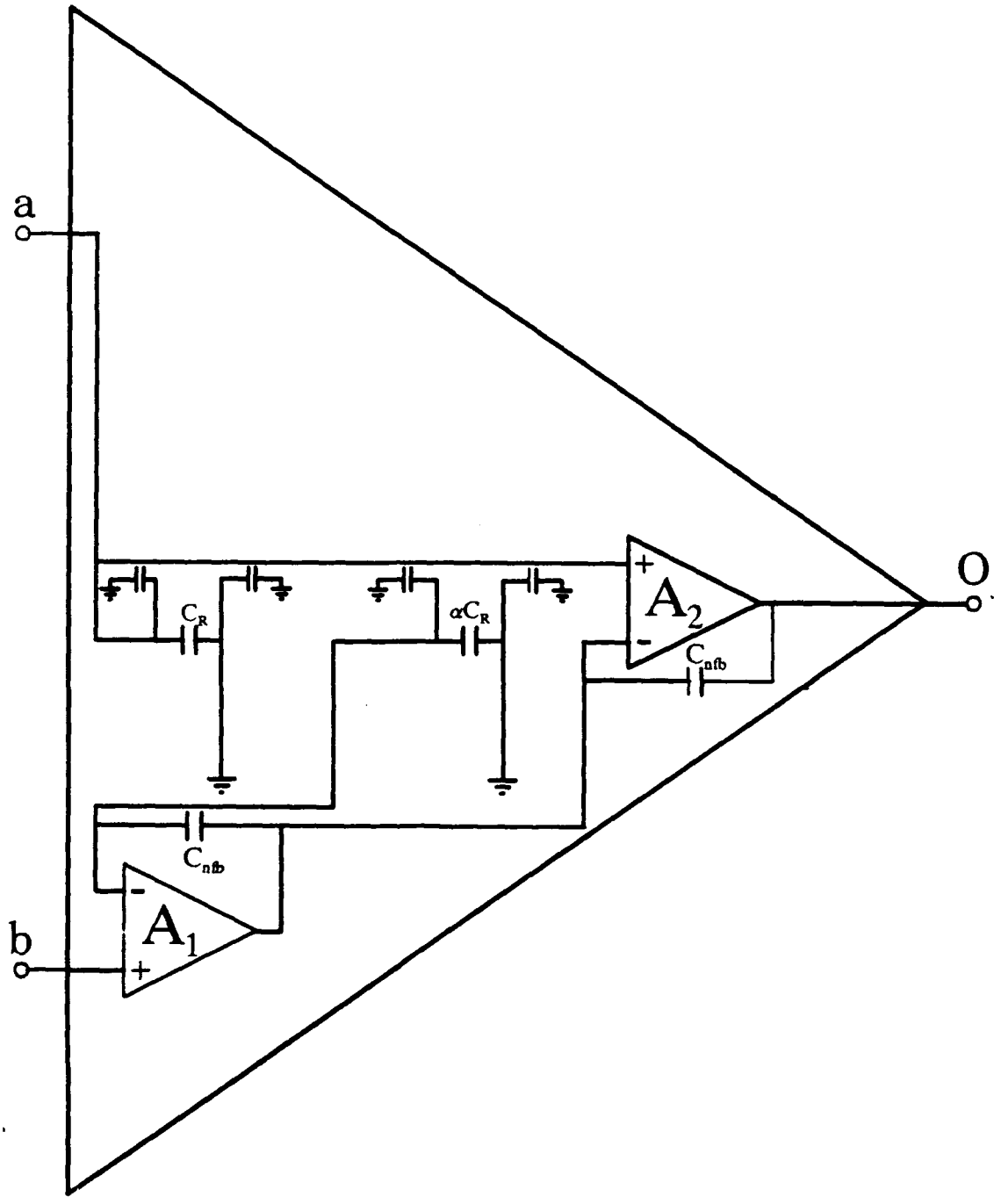

Figure 6.1f TSC C2OA-1 with Odd Phase Active

7. TSC C20A-1 with Φ_o Active and Effective Stray Capacitances

Figure 6.1g removes some of the stray capacitances from the design. This reduction in stray capacitances leaves only the effective stray capacitances with the Φ_o clock active. This reduction in stray capacitances uses the familiar criteria:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.
2. Capacitances between the output of an OA and ground are inconsequential.
3. Capacitances that are driven by a voltage source are inconsequential.

In this particular case, all stray capacitances that originated from the toggle switch capacitor implementation of C2OA-1 have been eliminated. These stray capacitances that were eliminated from the stray capacitances Φ_o clocked circuit will only be eliminated from the entire TSC C2OA-1 circuit if they can additionally be eliminated from the Φ_e clocked circuit.

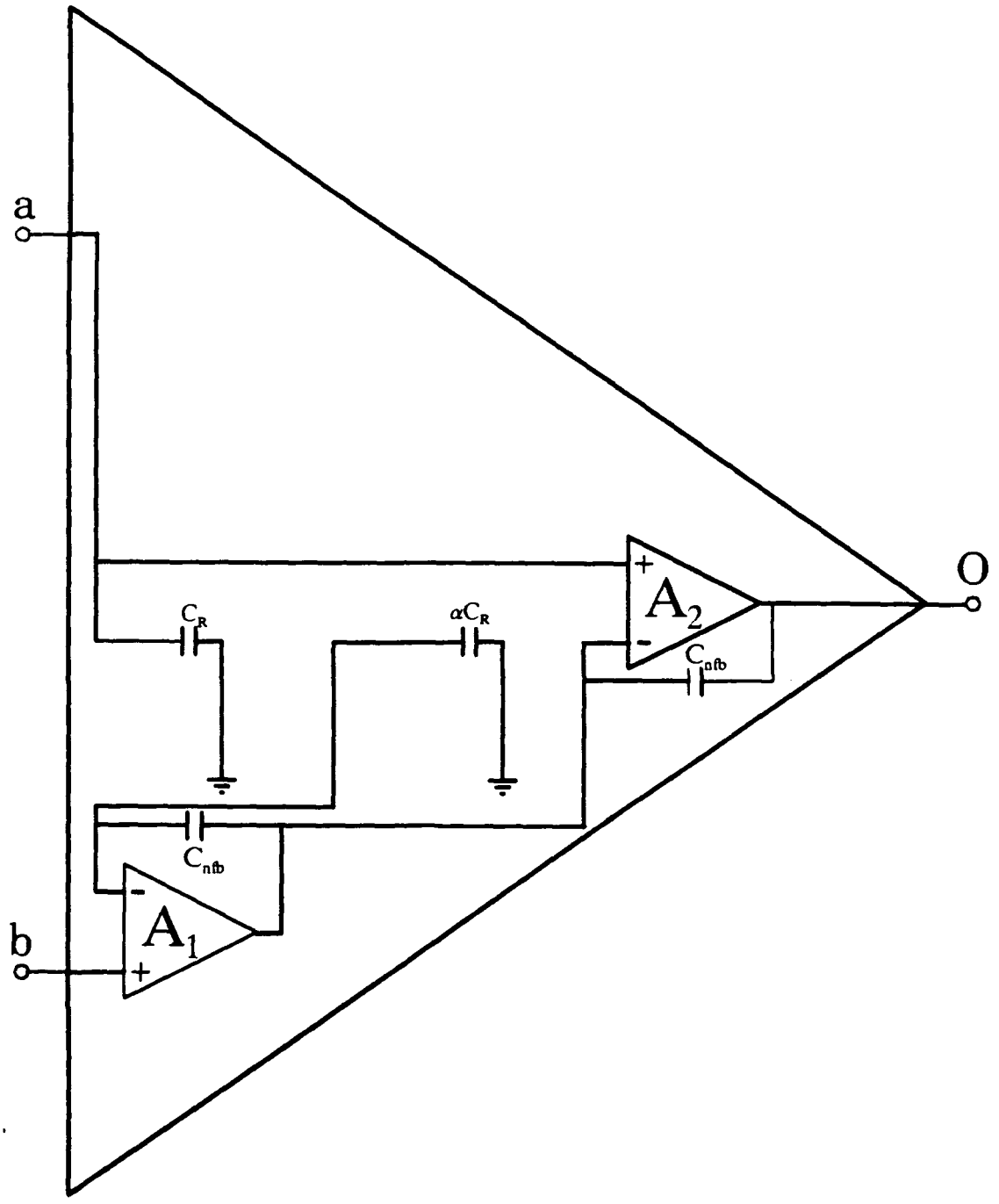

Figure 6.1g TSC C2OA-1 with Φ_o Active and Effective Stray Capacitances

8. TSC C2OA-1 with Even Phase Active

Figure 6.1h has the Φ_e clock active. This closes the four Φ_e switches and leaves the four Φ_o switches open and eliminates some of the circuit's complexity. The goal here is to ascertain which stray capacitances, if any, can be eliminated.

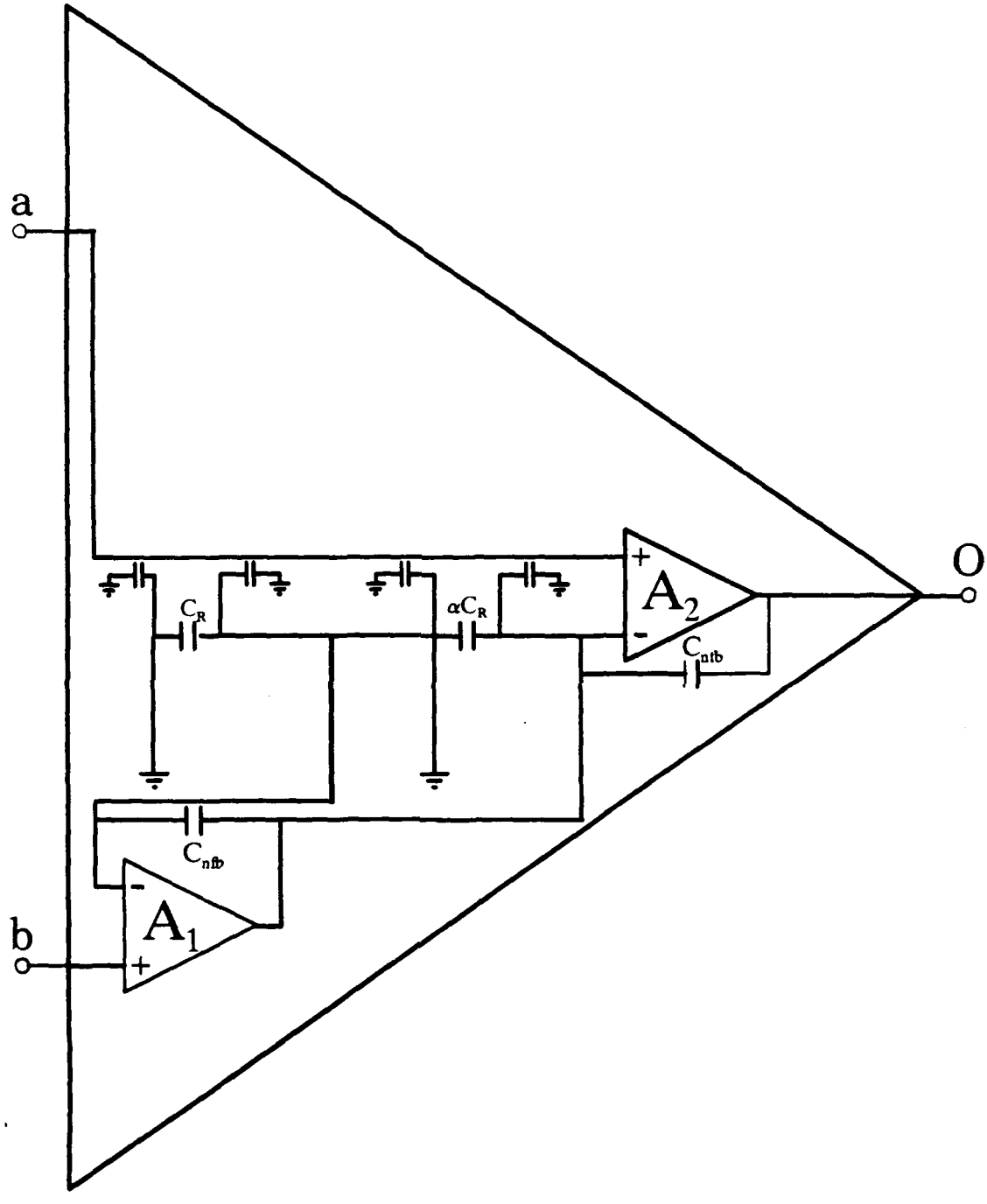

Figure 6.1h TSC C2OA-1 with Even Phase Active

9. TSC C20A-1 with Φ_e Active and Effective Stray Capacitances

Figure 6.1i removes some of the stray capacitances from the design. This reduction in stray capacitances leaves only the effective stray capacitances with the Φ_e clock active. This reduction in stray capacitances uses the familiar criteria:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.

2. Capacitances between the output of an OA and ground are inconsequential.

3. Capacitances that are driven by a voltage source are inconsequential.

In this particular case, all stray capacitances that originated from the toggle switch capacitor implementation of C2OA-1 have been eliminated. These stray capacitances that were eliminated from the stray capacitances Φ_e clocked circuit will be eliminated from the entire TSC C2OA-1 circuit because they were previously eliminated from the Φ_o clocked circuit.

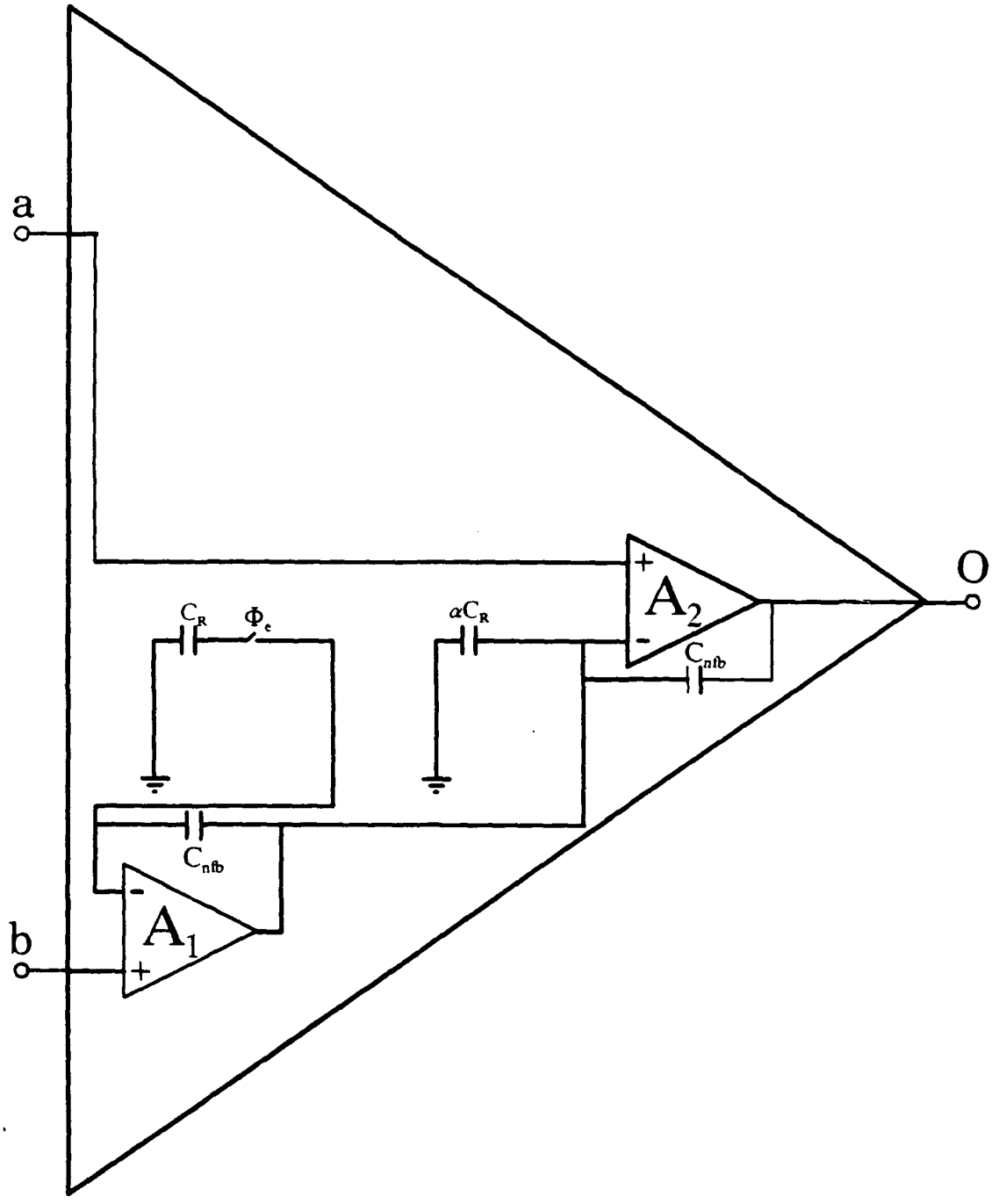

Figure 6.1i TSC C2OA-1 with Φ_e Active and Effective Stray Capacitances

10. Stray Insensitive TSC C2OA-1

Figure 6.1j depicts the final TSC C2OA-1 circuit. This circuit will be implemented as the first design in this thesis. This circuit is only missing the two phase nonoverlapping clock design for completeness, but the actual design for this clock was shown in Chapter IV. The wiring diagram for this circuit as well as the wiring diagram for the two phase nonoverlapping clock will be shown in Chapter VII.

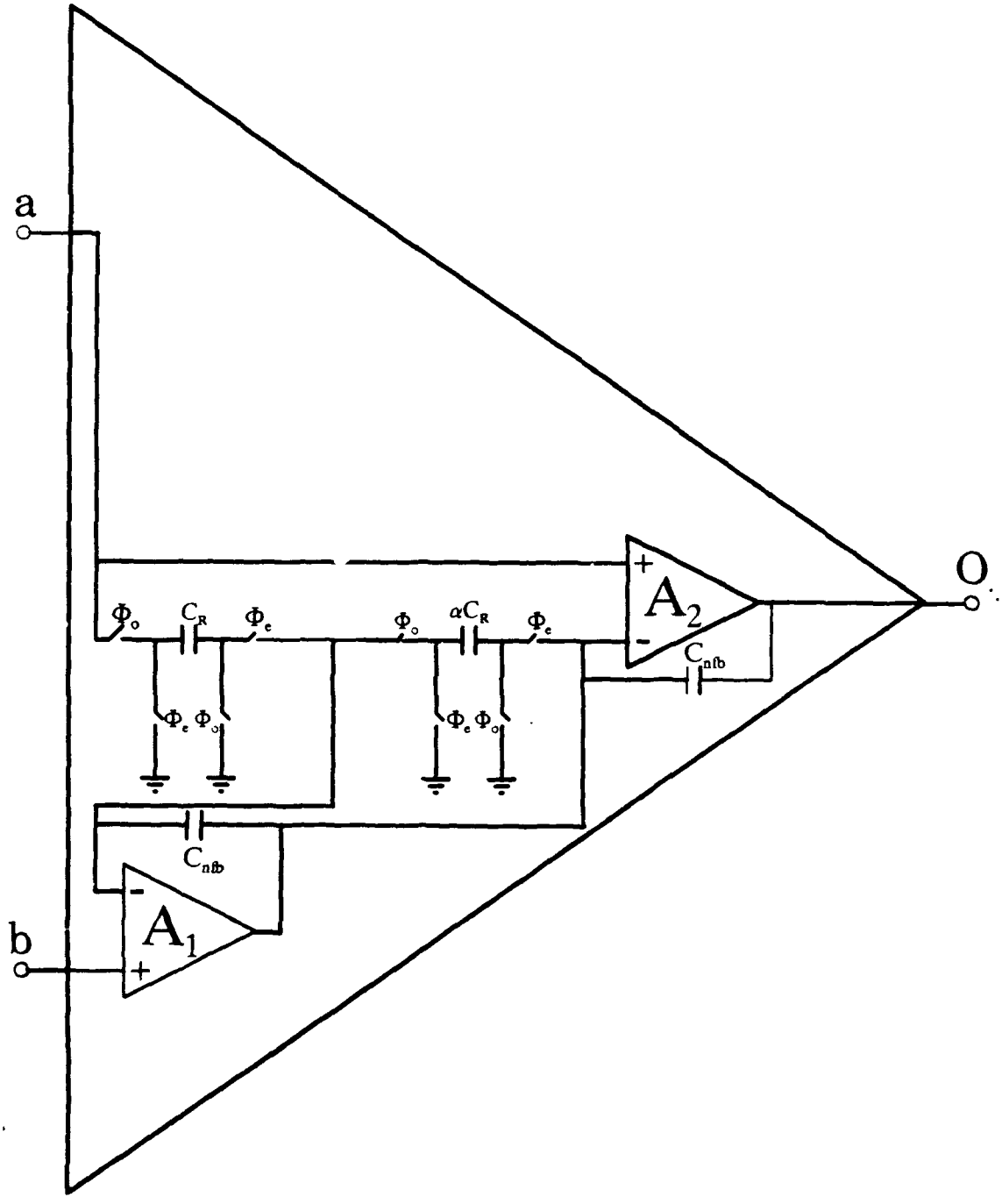

Figure 6.1j Stray Insensitive TSC C2OA-1

C. TOGGLE SWITCH CAPACITOR C2OA-2

1. C2OA-2

Figure 6.2a on the next page depicts C2OA-2 in its original form as designed from nullator and norator modeling and having passed the four required performance criteria as set forth in Chapter III. The three-terminal equivalent is shown to the upper right.

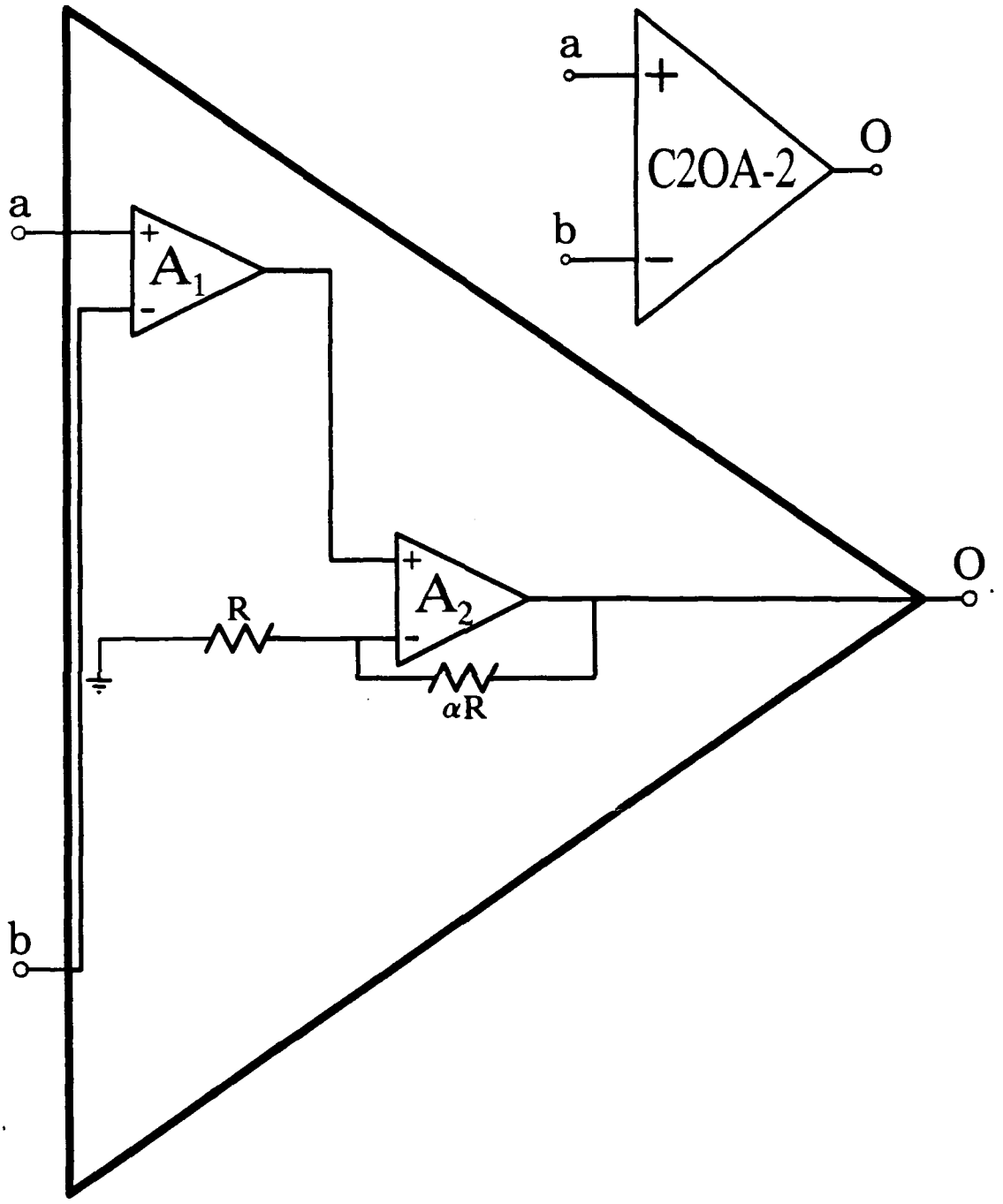

Figure 6.2a C2OA-2

2. TSC C2OA-2

Figure 6.2b realizes the toggle switched capacitor equivalent for the two resistors from the basic C2OA-2 form. Chapter IV detailed this transformation. In order to avoid nonlinearities and saturation, two capacitors, labeled C_{nb} , were added.

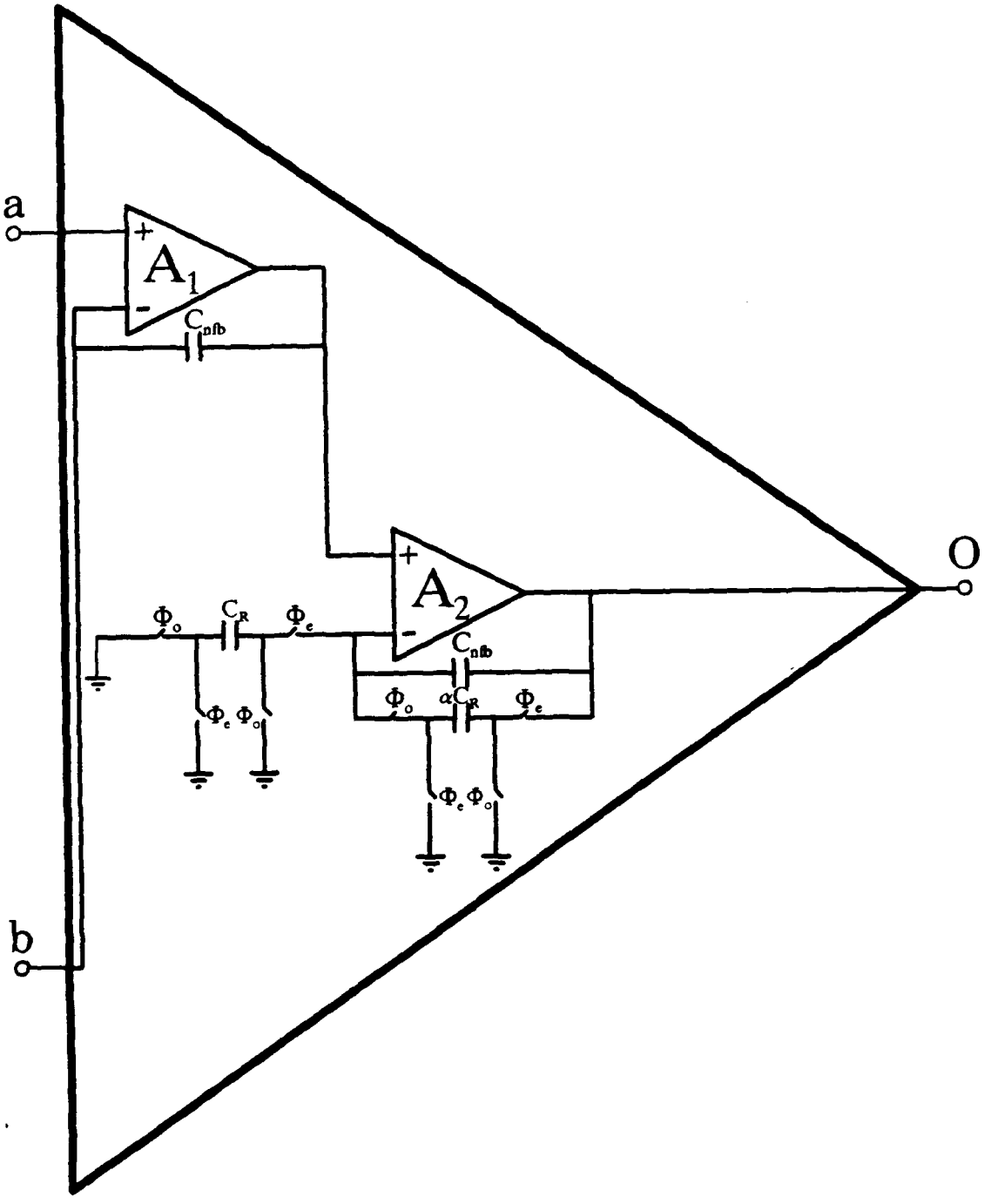

Figure 6.2b TSC C2OA-2

3. TSC C2OA-2 with Stray Capacitances

Figure 6.2c reflects the design with all possible stray capacitances added to the circuit as discussed in Chapter V. Not all of these stray capacitances actually exist, nor will all of them remain in the circuit if the design is well made. A good switched capacitor design will remove most, if not all, of the stray capacitances that were artificially introduced in the design.

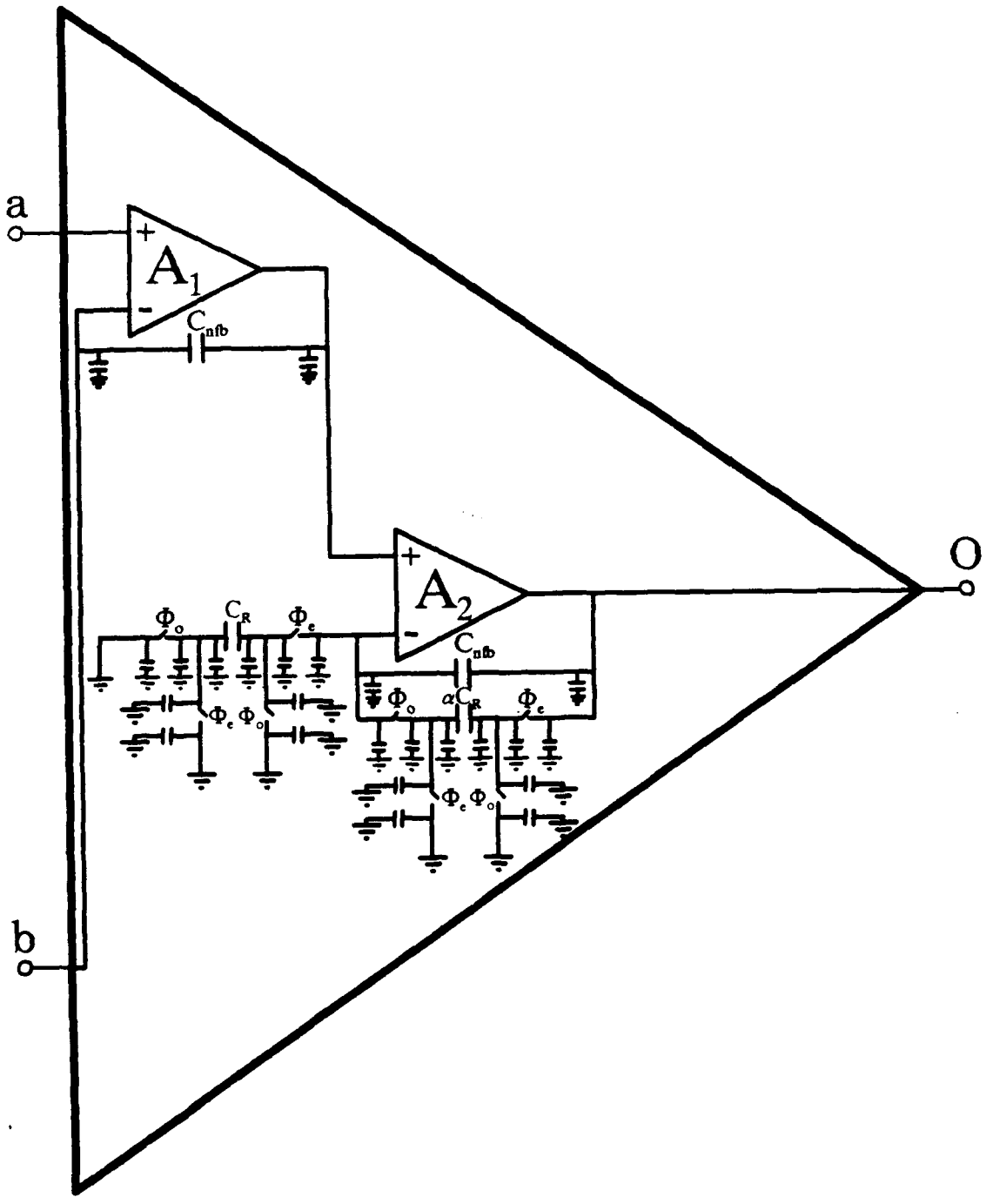

Figure 6.2c TSC C2OA-2 with Stray Capacitances

4. TSC C2OA-2 with Combined Stray Capacitances

Figure 6.2d combines the stray capacitances at each node into a single stray capacitance in order to simplify the circuit. The combined capacitors have been placed in the figure at a different position than any of the uncombined capacitors previously held so that they might present themselves more readily.

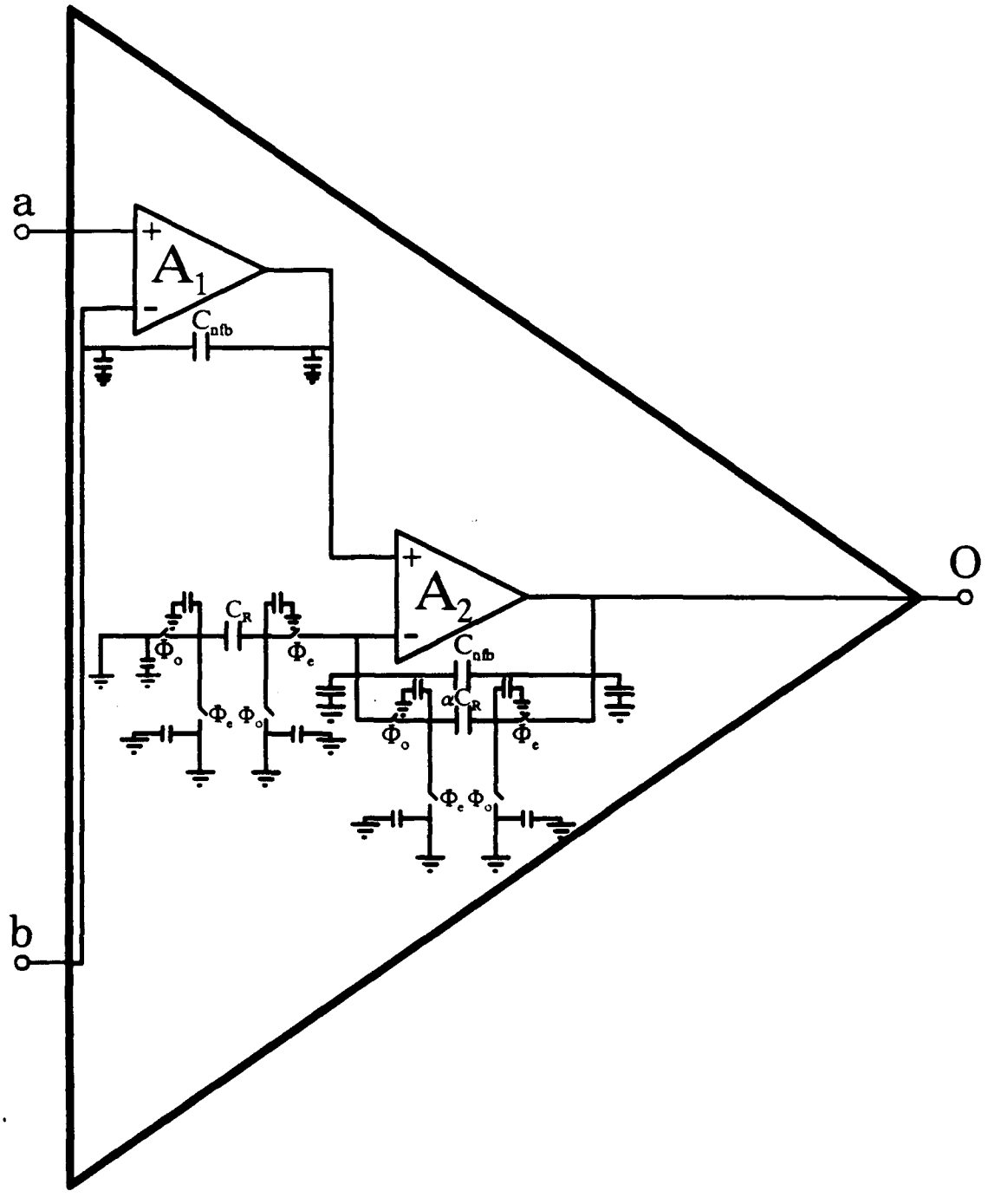

Figure 6.2d TSC C2OA-2 with Combined Stray Capacitances

5. TSC C2OA-2 with Reduced Stray Capacitances

Figure 6.2e removes some of the stray capacitances from the design. This reduction in stray capacitances was detailed in Chapter V and is summarized here below:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.

2. Capacitances between the output of an OA and ground are inconsequential.

3. Capacitances that are driven by a voltage source are inconsequential.

The remaining stray capacitances are not necessarily effective stray capacitances. The TSC topology must first be allowed to further reduce these parasitic capacitances.

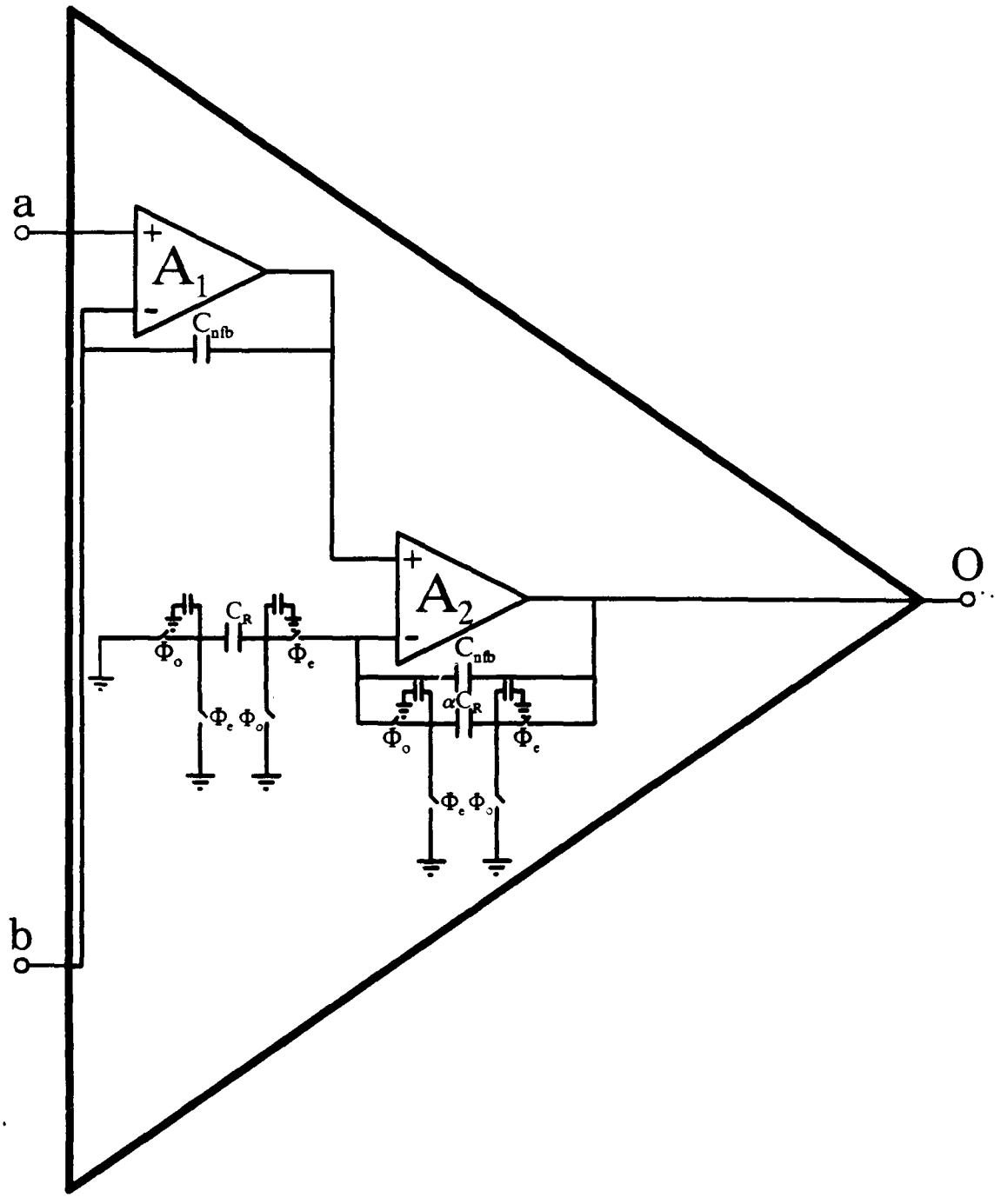

Figure 6.2e TSC C2OA-2 with Reduced Stray Capacitances

6. TSC C2OA-2 with Odd Phase Active

Figure 6.2f has the Φ_o clock active. This closes the four Φ_o switches and leaves the four Φ_e switches open and eliminates some of the circuit's complexity. The goal here is to ascertain which stray capacitances, if any, can be eliminated.

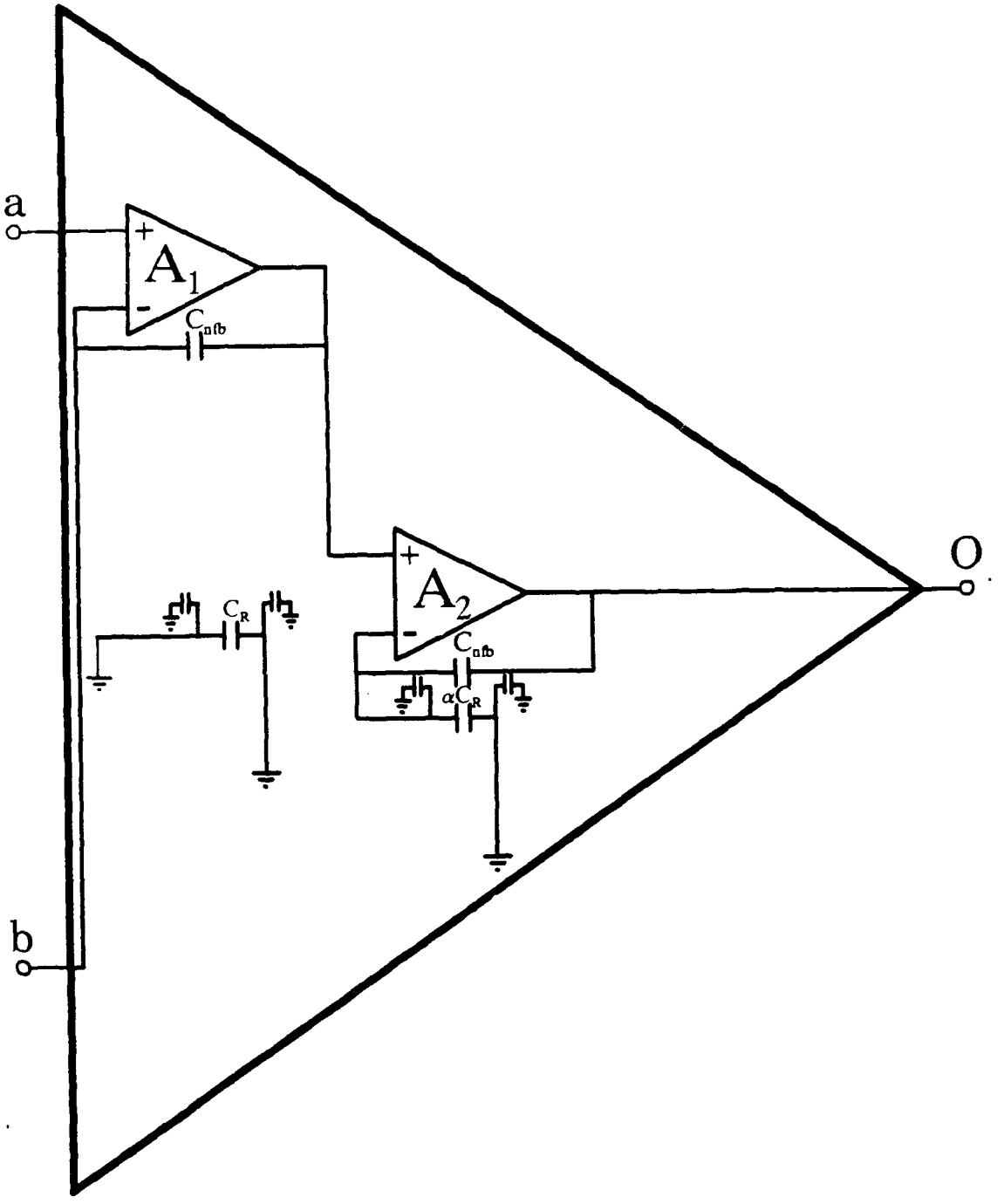

Figure 6.2f TSC C2OA-2 with Odd Phase Active

7. TSC C20A-2 with Φ_o Active and Effective Stray Capacitances

Figure 6.2g removes some of the stray capacitances from the design. This reduction in stray capacitances leaves only the effective stray capacitances with the Φ_o clock active. This reduction in stray capacitances uses the familiar criteria:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.

2. Capacitances between the output of an OA and ground are inconsequential.

3. Capacitances that are driven by a voltage source are inconsequential.

In this particular case, all stray capacitances that originated from the toggle switch capacitor implementation of C2OA-2 have been eliminated. These stray capacitances that were eliminated from the stray capacitances Φ_o clocked circuit will only be eliminated from the entire TSC C2OA-2 circuit if they can additionally be eliminated from the Φ_e clocked circuit.

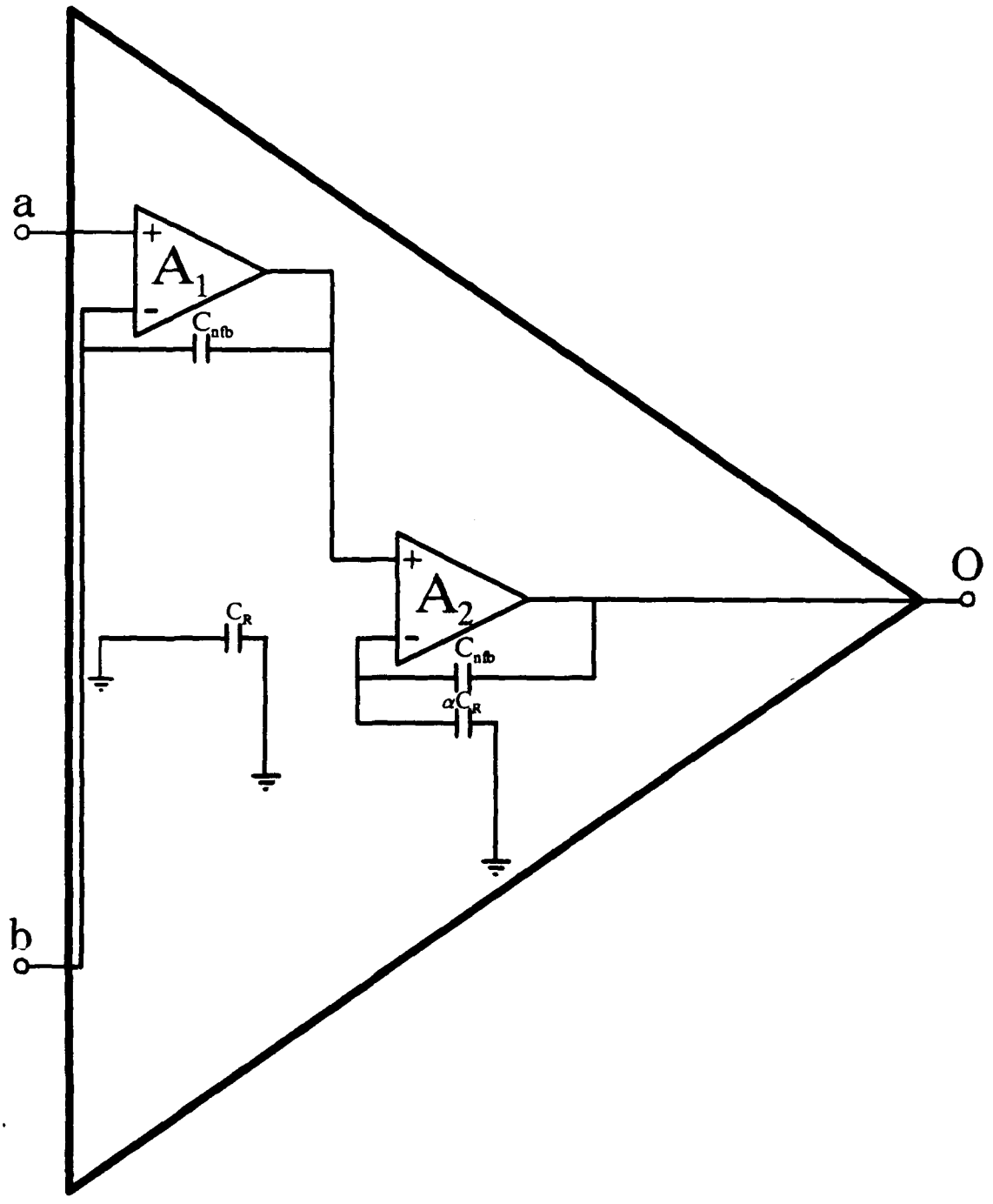

Figure 6.2g TSC C2OA-2 with Φ_o Active and Effective Stray Capacitances

8. TSC C2OA-2 with Even Phase Active

Figure 6.2h has the Φ_e clock active. This closes the four Φ_e switches and leaves the four Φ_o switches open and eliminates some of the circuit's complexity. The goal here is to ascertain which stray capacitances, if any, can be eliminated.

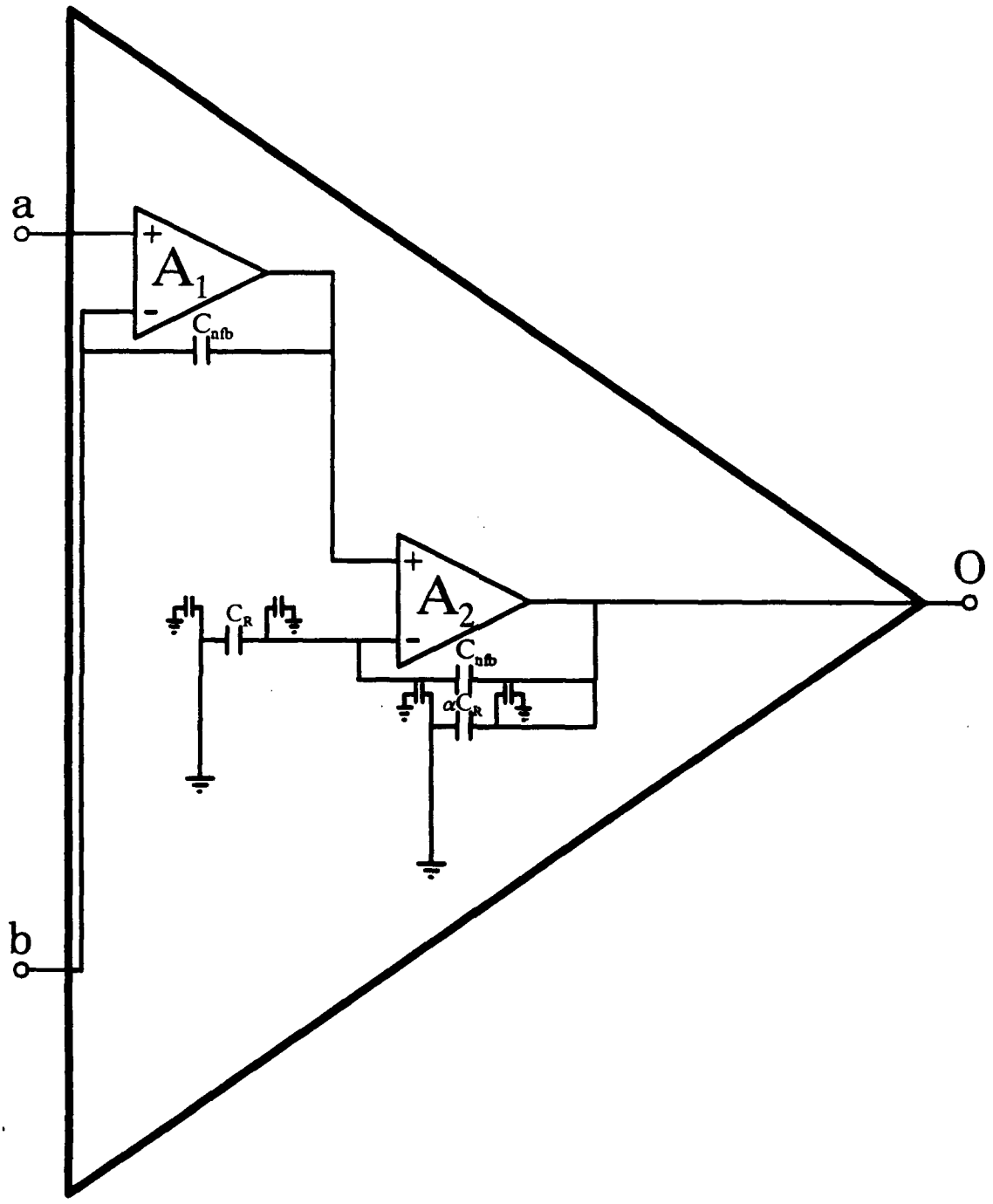

Figure 6.2h TSC C2OA-2 with Even Phase Active

9. TSC C2OA-2 with Φ_e Active and Effective Stray Capacitances

Figure 6.2i removes some of the stray capacitances from the design. This reduction in stray capacitances leaves only the effective stray capacitances with the Φ_e clock active. This reduction in stray capacitances uses the familiar criteria:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.
2. Capacitances between the output of an OA and ground are inconsequential.
3. Capacitances that are driven by a voltage source are inconsequential.

In this particular case, all stray capacitances that originated from the toggle switch capacitor implementation of C2OA-2 have been eliminated. These stray capacitances that were eliminated from the stray capacitances Φ_e clocked circuit will be eliminated from the entire TSC C2OA-2 circuit because they were previously eliminated from the Φ_o clocked circuit.

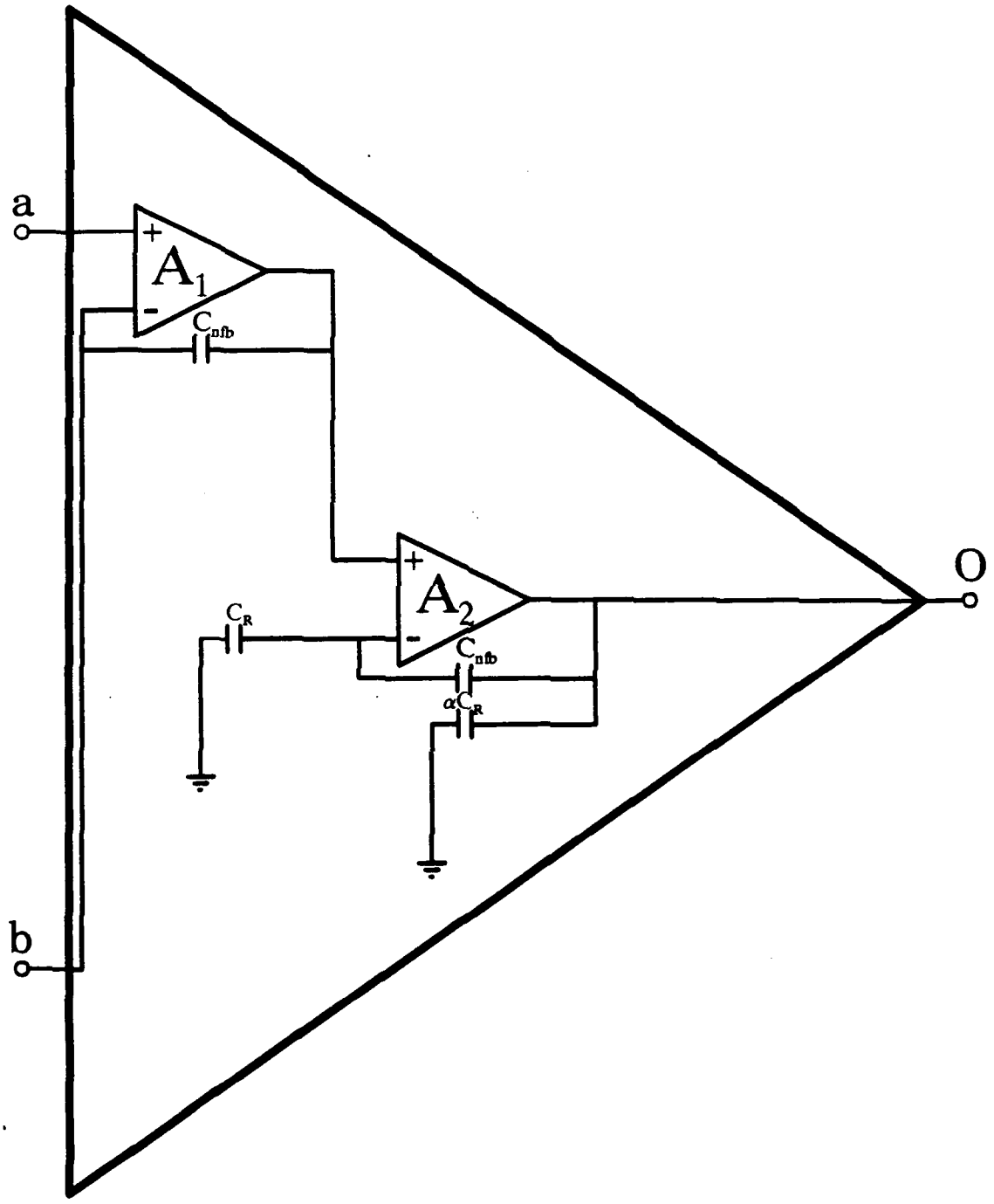

Figure 6.2i TSC C2OA-2 with Φ_e Active and Effective Stray Capacitances

10. Stray Insensitive TSC C2OA-2

Figure 6.2j depicts the final TSC C2OA-2 circuit. This circuit will be implemented as the second design in this thesis. This circuit is missing only the two phase nonoverlapping clock design for completeness, but the actual design for this clock was shown in Chapter IV. The wiring diagram for this circuit as well as the wiring diagram for the two phase nonoverlapping clock will be shown in Chapter VII.

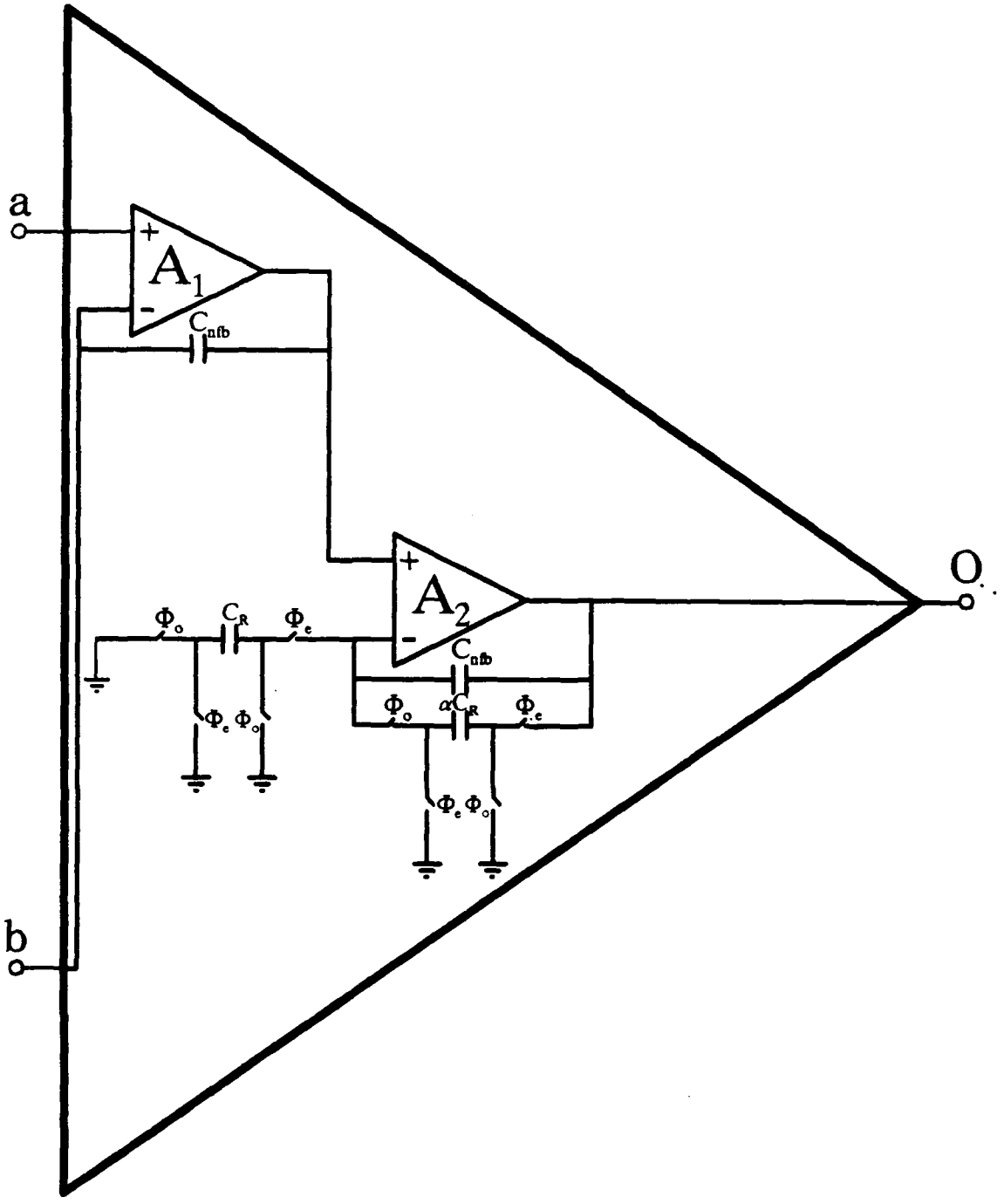

Figure 6.2j Stray Insensitive TSC C2OA-2

D. MODIFIED OPEN-CIRCUIT FLOATING RESISTOR C20A-1

1. C2OA-1

Figure 6.3a on the next page depicts C2OA-1 in its original form as designed from nullator and norator modeling and having passed the four required performance criteria as set forth in Chapter III. The three-terminal equivalent is shown to the upper right.

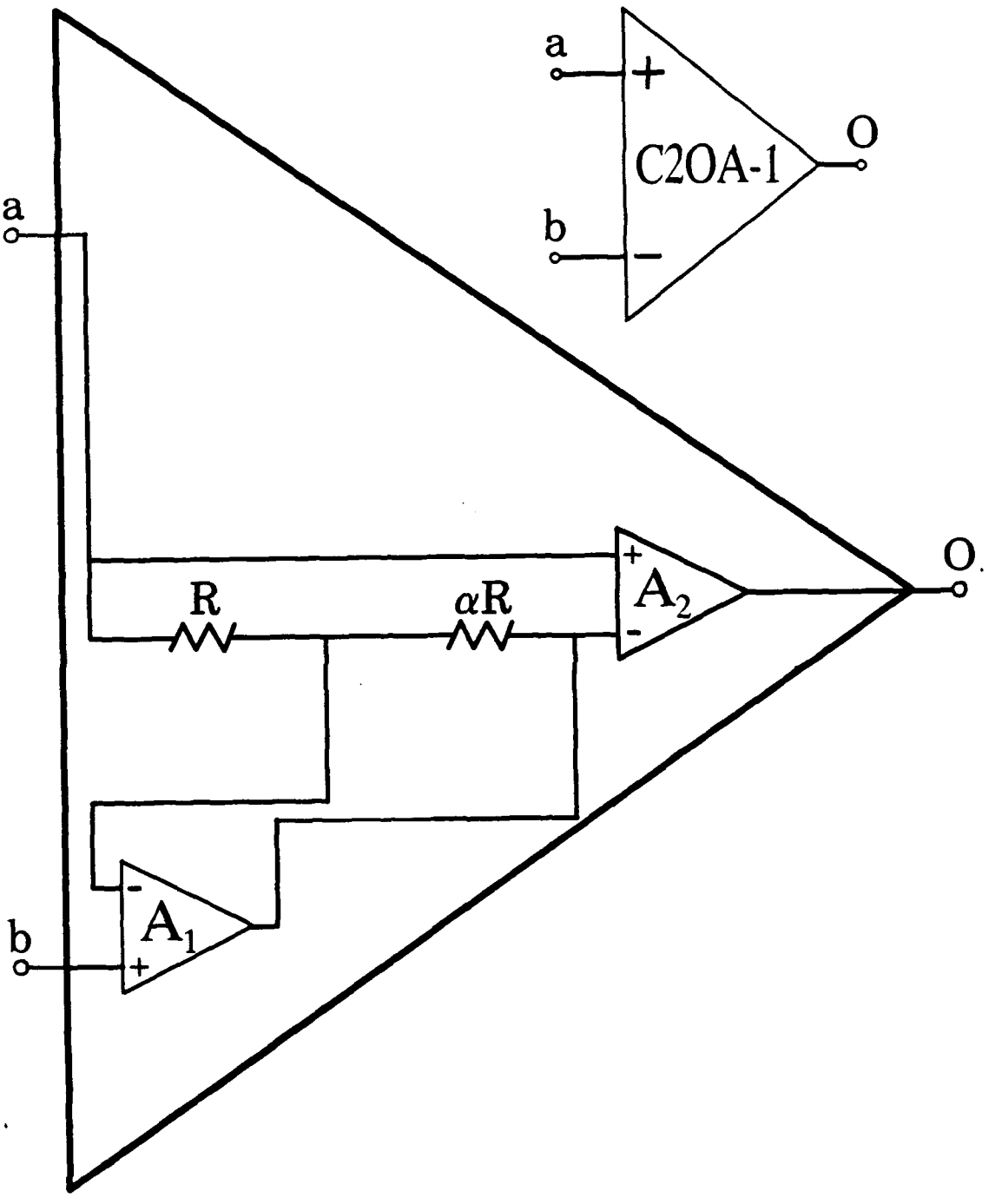

Figure 6.3a C20A-1

2. MOFR C2OA-1

Figure 6.3b realizes the modified open-circuit floating resistor equivalent for the two resistors from the basic C2OA-1 form. Chapter IV detailed this transformation. In order to avoid nonlinearities and saturation, two capacitors, labeled C_{nfb}, were added.

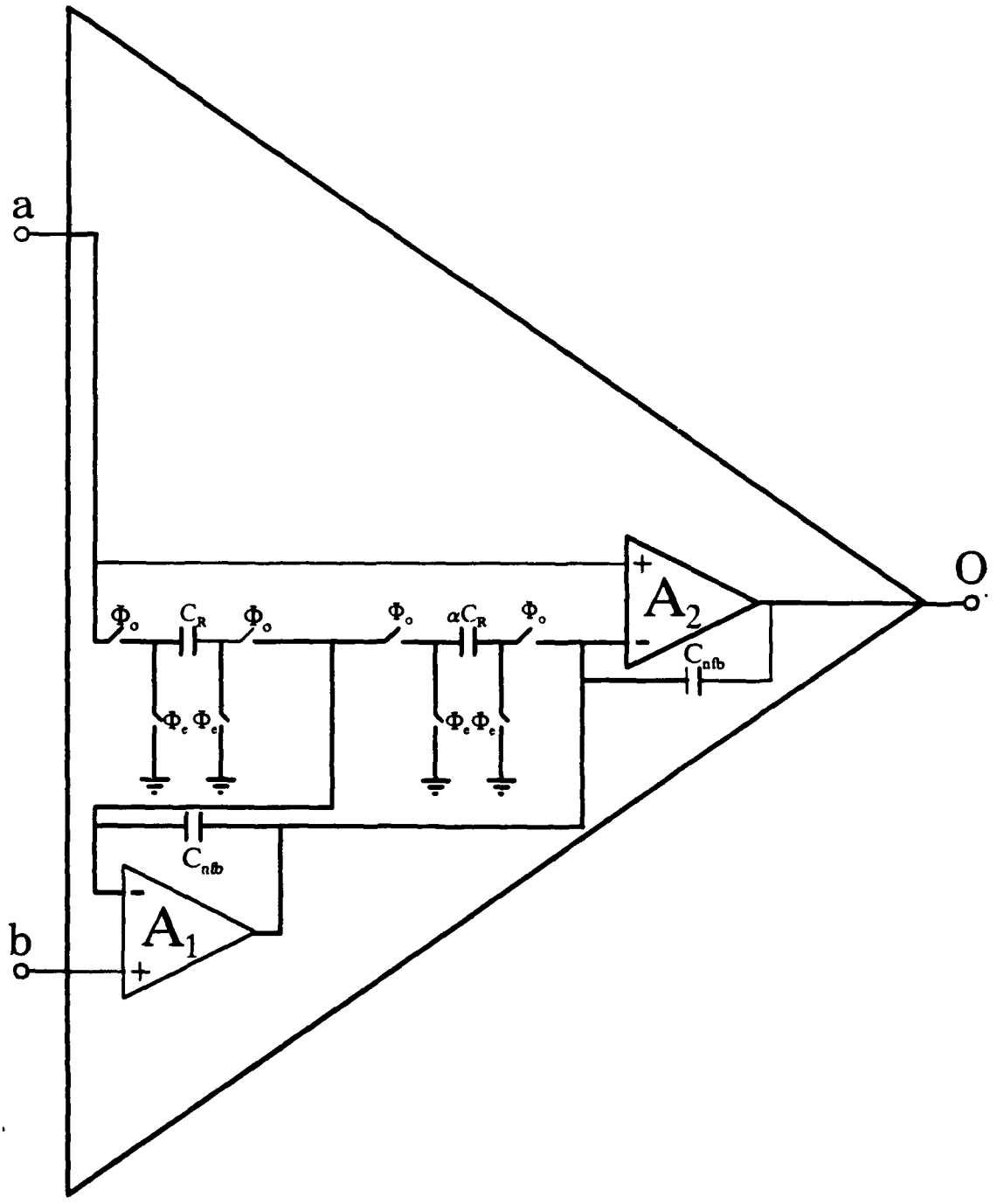

Figure 6.3b MOFR C2OA-1

3. MOFR C2OA-1 with Stray Capacitances

Figure 6.3c reflects the design with all possible stray capacitances added to the circuit as discussed in Chapter V. Not all of these stray capacitances actually exist, nor will all of them remain in the circuit if the design is well made. A good switched capacitor design will remove most, if not all, of the stray capacitances that were artificially introduced in the design.

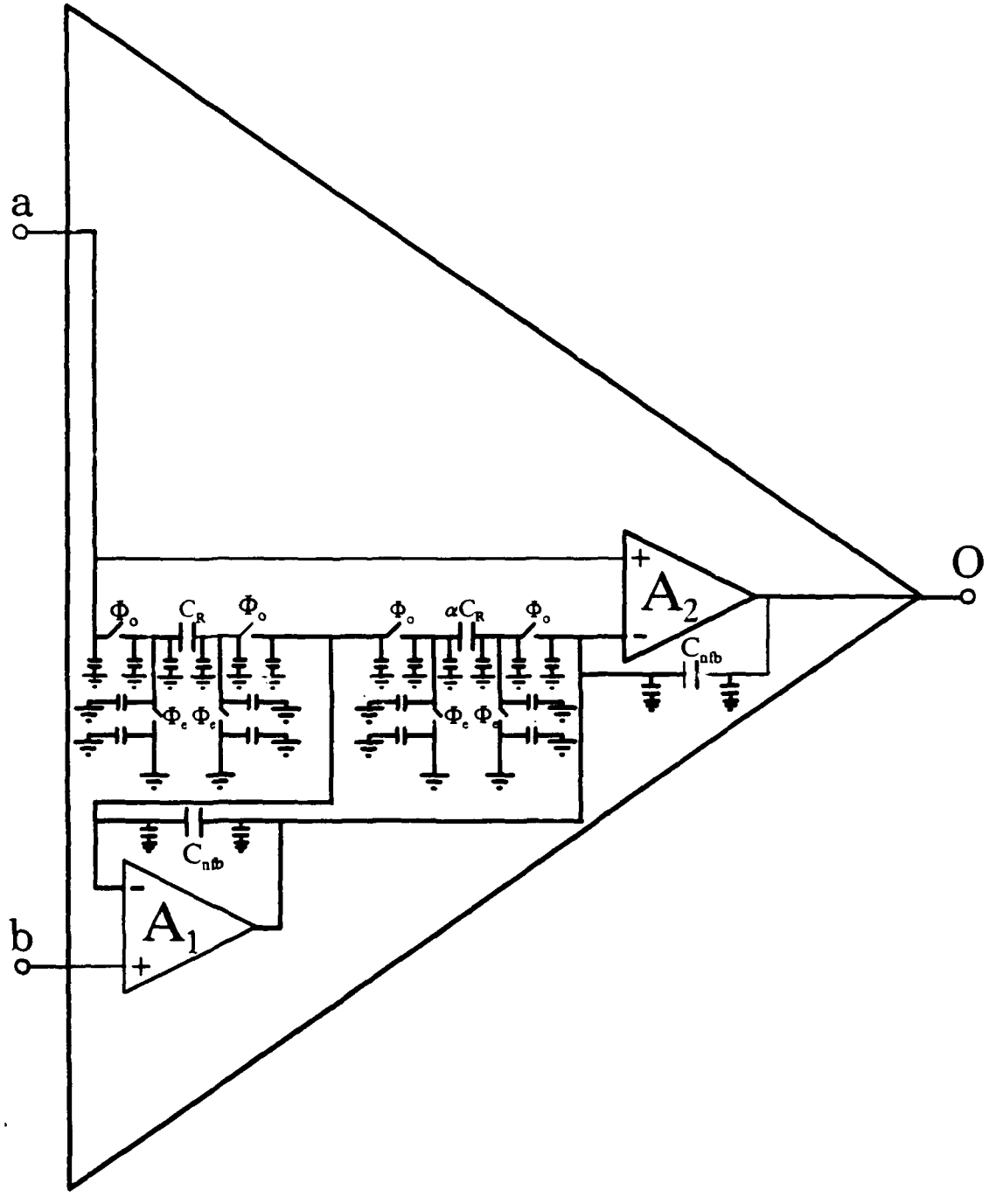

Figure 6.3c MOFR C2OA-1 with Stray Capacitances

4. MOFR C2OA-1 with Combined Stray Capacitances

Figure 6.3d combines the stray capacitances at each node into a single stray capacitance in order to simplify the circuit. The combined capacitors have been placed in the figure at a different position than any of the uncombined capacitors previously held so that they might present themselves more readily.

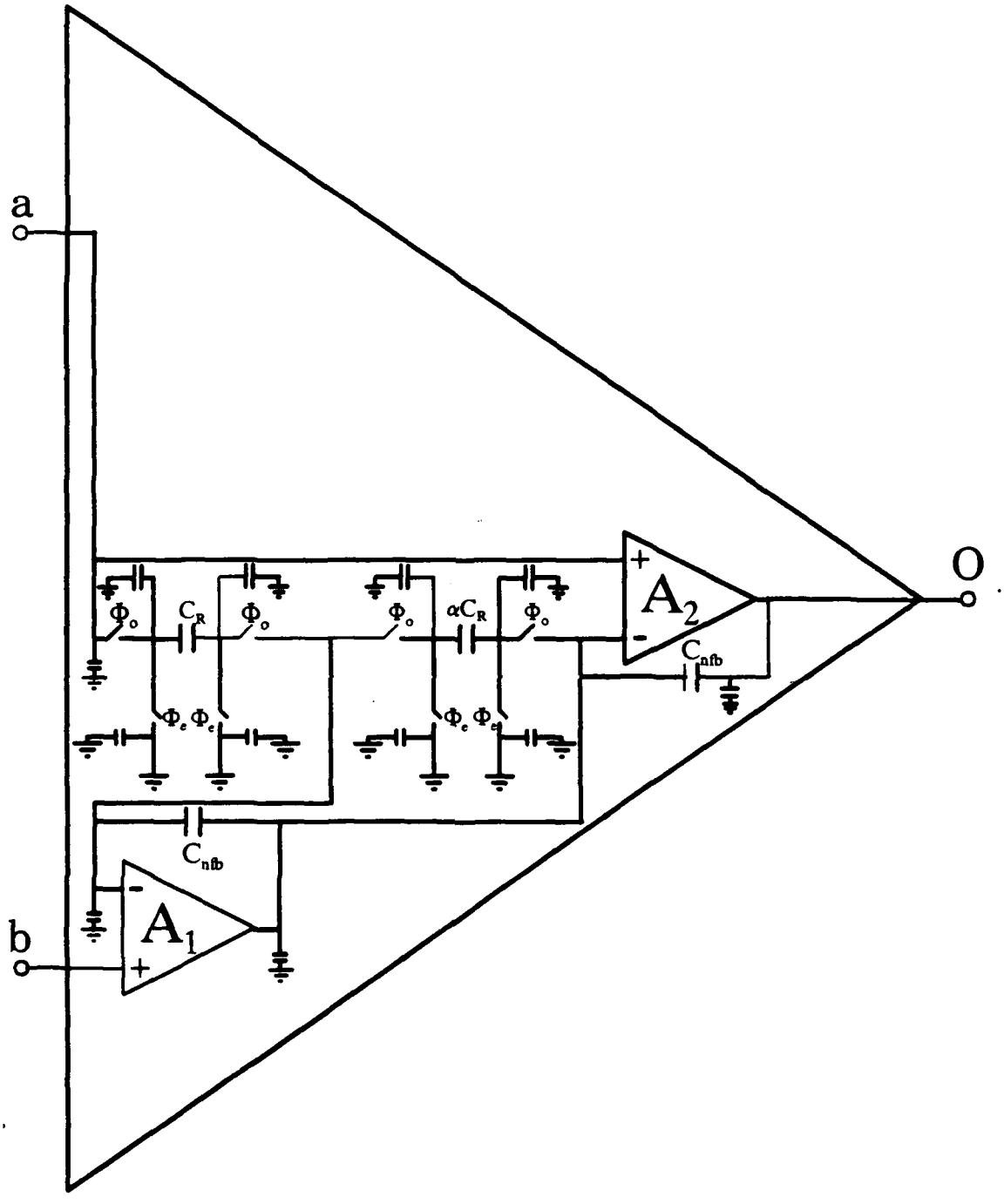

Figure 6.3d MOFR C2OA-1 with Combined Stray Capacitances

5. MOFR C2OA-1 with Reduced Stray Capacitances

Figure 6.3e removes some of the stray capacitances from the design. This reduction in stray capacitances was detailed in Chapter V and is summarized below:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.

2. Capacitances between the output of an OA and ground are inconsequential.

3. Capacitances that are driven by a voltage source are inconsequential.

The remaining stray capacitances are not necessarily effective stray capacitances. The mOFR topology must first be allowed to further reduce these parasitic capacitances.

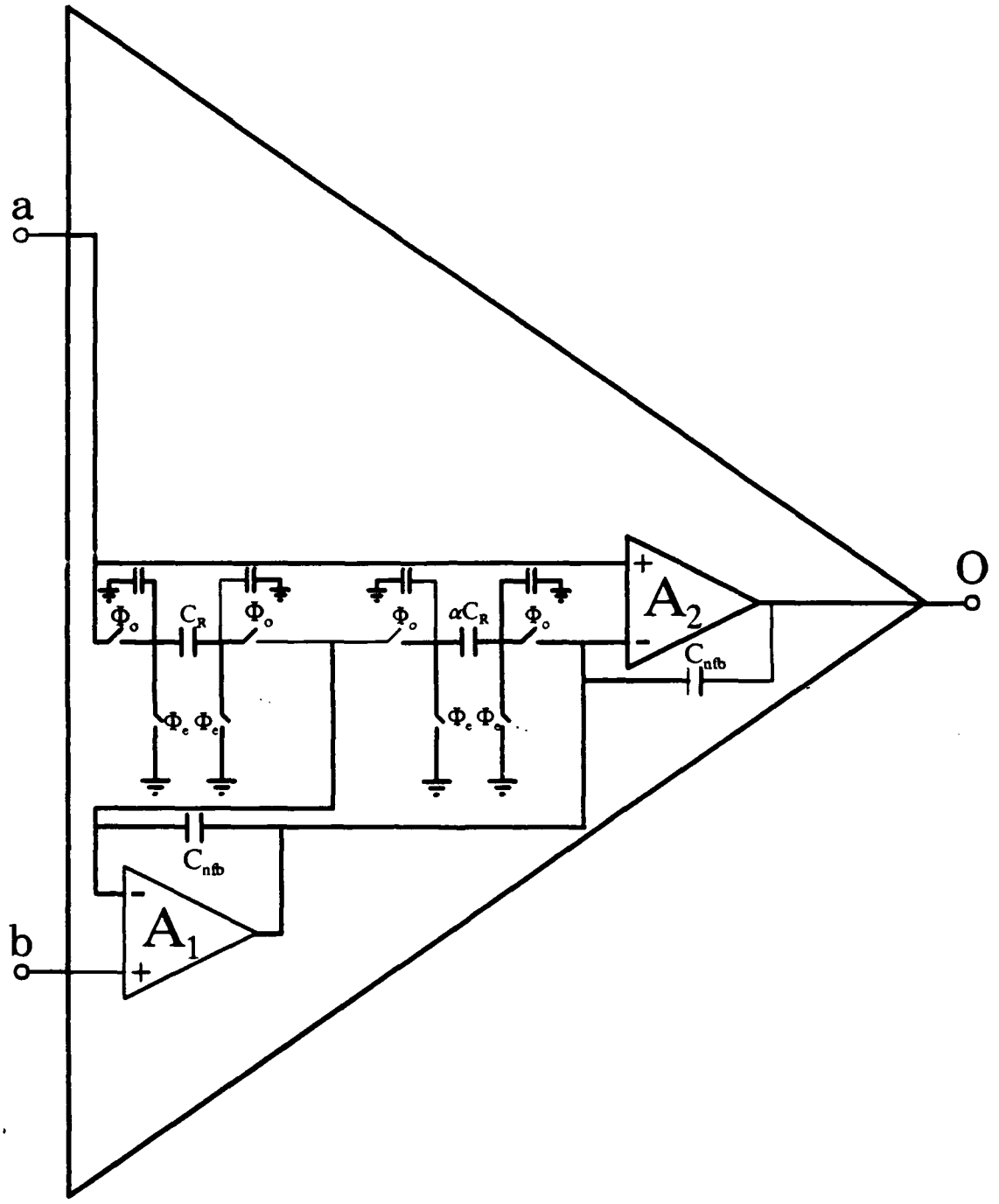

Figure 6.3e MOFR C2OA-1 with Reduced Stray Capacitances

6. MOFR C2OA-1 with Odd Phase Active

Figure 6.3f has the Φ_o clock active. This closes the four Φ_o switches and leaves the four Φ_e switches open and eliminates some of the circuit's complexity. The goal here is to ascertain which stray capacitances, if any, can be eliminated.

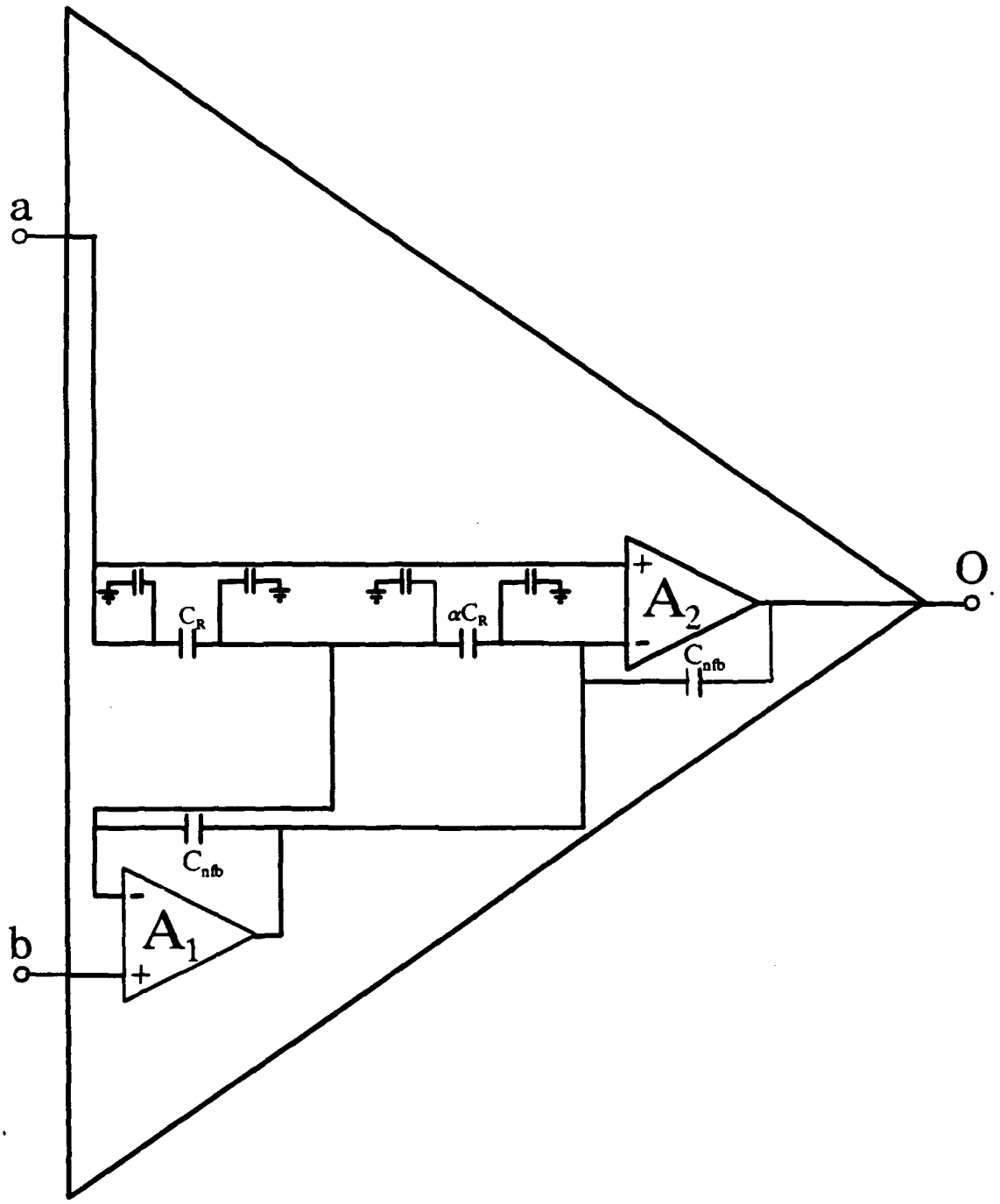

Figure 6.3f MOFR C2OA-1 with Odd Phase Active

7. MOFR C2OA-1 with Φ_o Active and Effective Stray Capacitances

Figure 6.3g removes some of the stray capacitances from the design. This reduction in stray capacitances leaves only the effective stray capacitances with the Φ_o clock active. This reduction in stray capacitances uses the familiar criteria:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.
2. Capacitances between the output of an OA and ground are inconsequential.
3. Capacitances that are driven by a voltage source are inconsequential.

In this particular case, all stray capacitances that originated from the modified open-circuit floating resistor implementation of C2OA-1 have been eliminated. These stray capacitances that were eliminated from the stray capacitances Φ_o clocked circuit will only be eliminated from the entire mOFR C2OA-1 circuit if they can additionally be eliminated from the Φ_e clocked circuit.

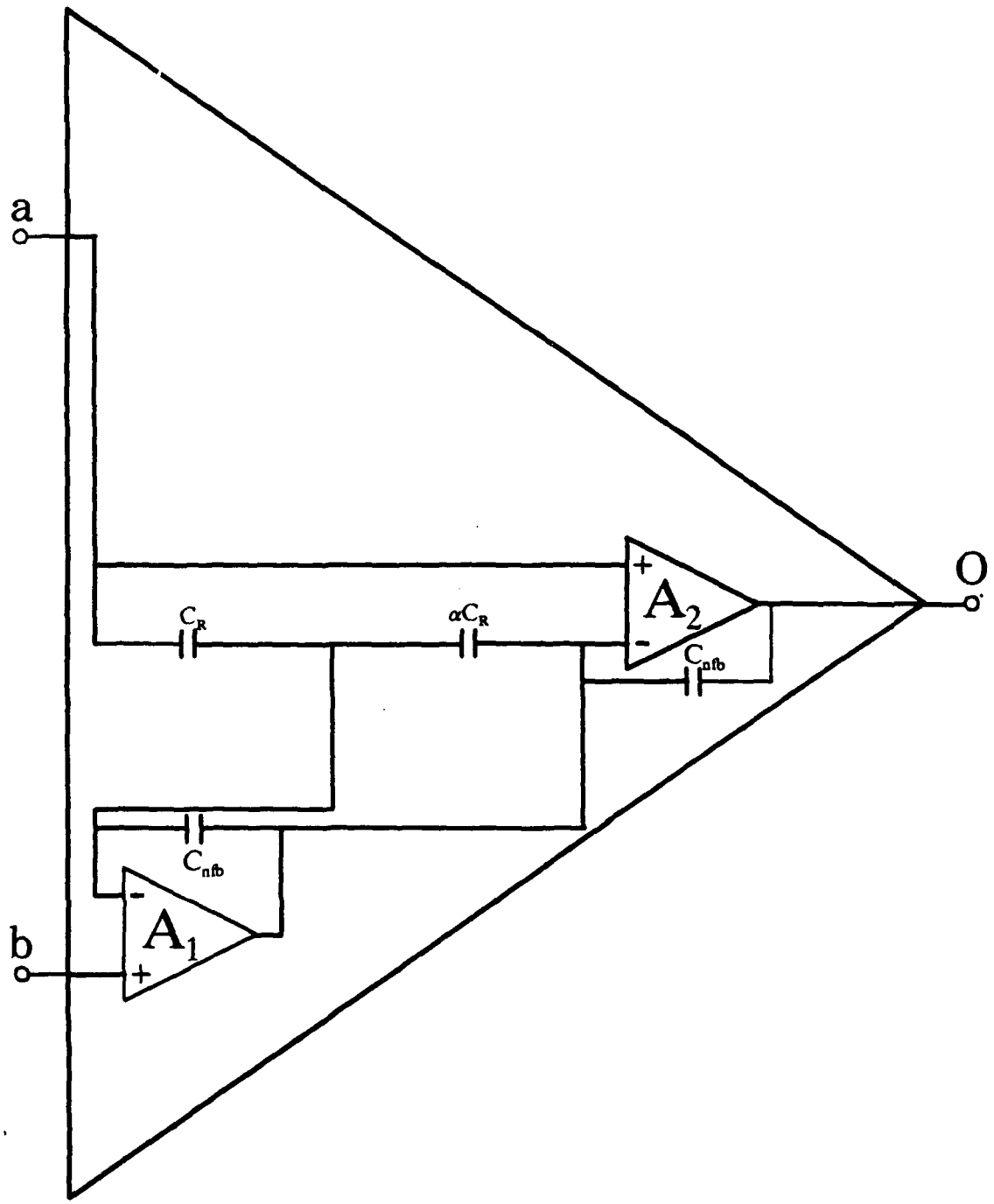

Figure 6.3g MOFR C2OA-1 with Φ_o Active and Effective Stray Capacitances

8. MOFR C2OA-1 with Even Phase Active

Figure 6.3h has the Φ_e clock active. This closes the four Φ_e switches and leaves the four Φ_o switches open and eliminates some of the circuit's complexity. The goal here is to ascertain which stray capacitances, if any, can be eliminated.

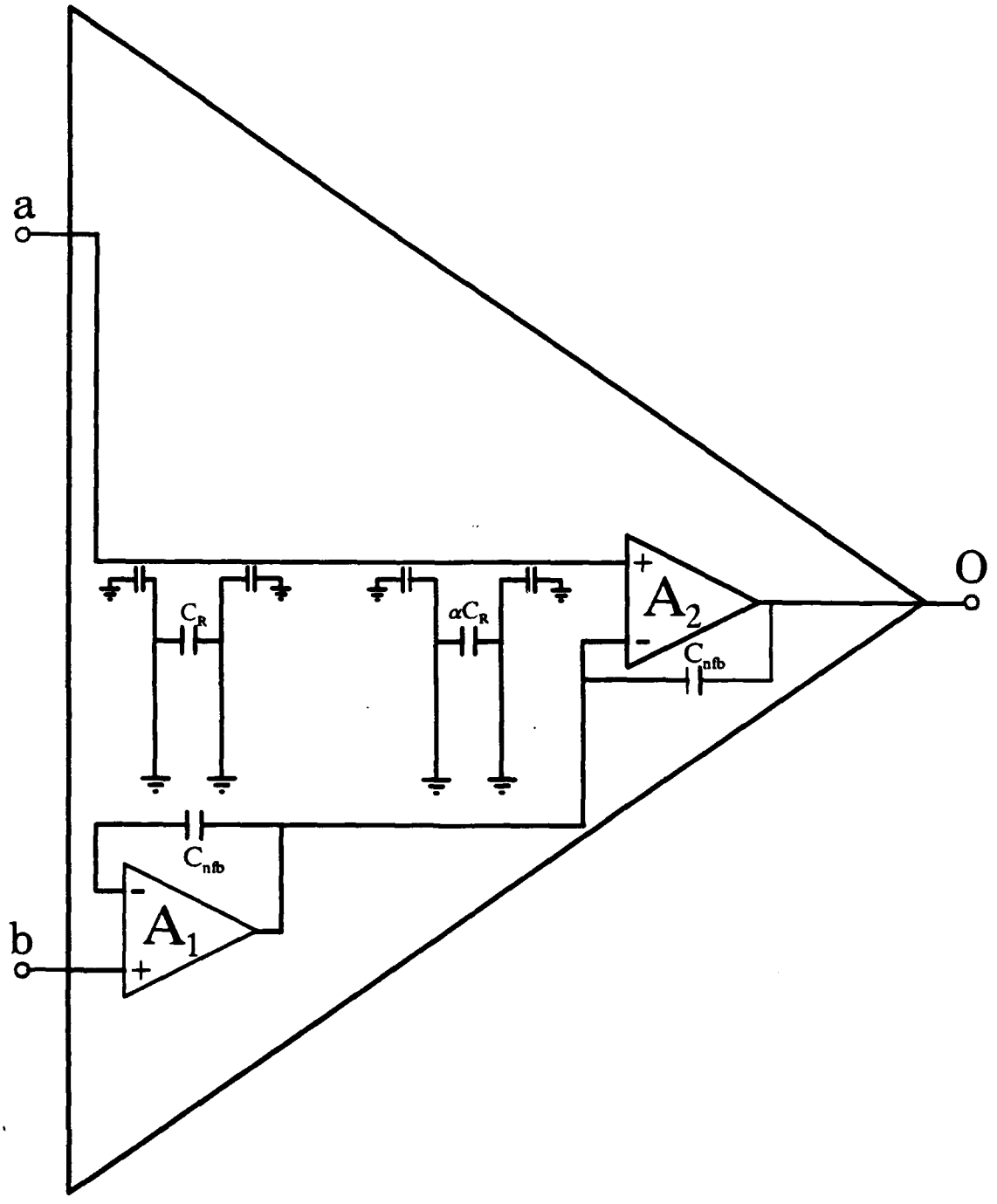

Figure 6.3h MOFR C2OA-1 with Even Phase Active

9. MOFR C2OA-1 with Φ_e Active and Effective Stray Capacitances

Figure 6.3i removes some of the stray capacitances from the design. This reduction in stray capacitances leaves only the effective stray capacitances with the Φ_e clock active. This reduction in stray capacitances uses the familiar criteria:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.
2. Capacitances between the output of an OA and ground are inconsequential.
3. Capacitances that are driven by a voltage source are inconsequential.

In this particular case, all stray capacitances that originated from the modified open-circuit floating resistor implementation of C2OA-1 have been eliminated. These stray capacitances that were eliminated from the stray capacitances Φ_e clocked circuit will be eliminated from the entire mOFR C2OA-1 circuit because they were previously eliminated from the Φ_o clocked circuit.

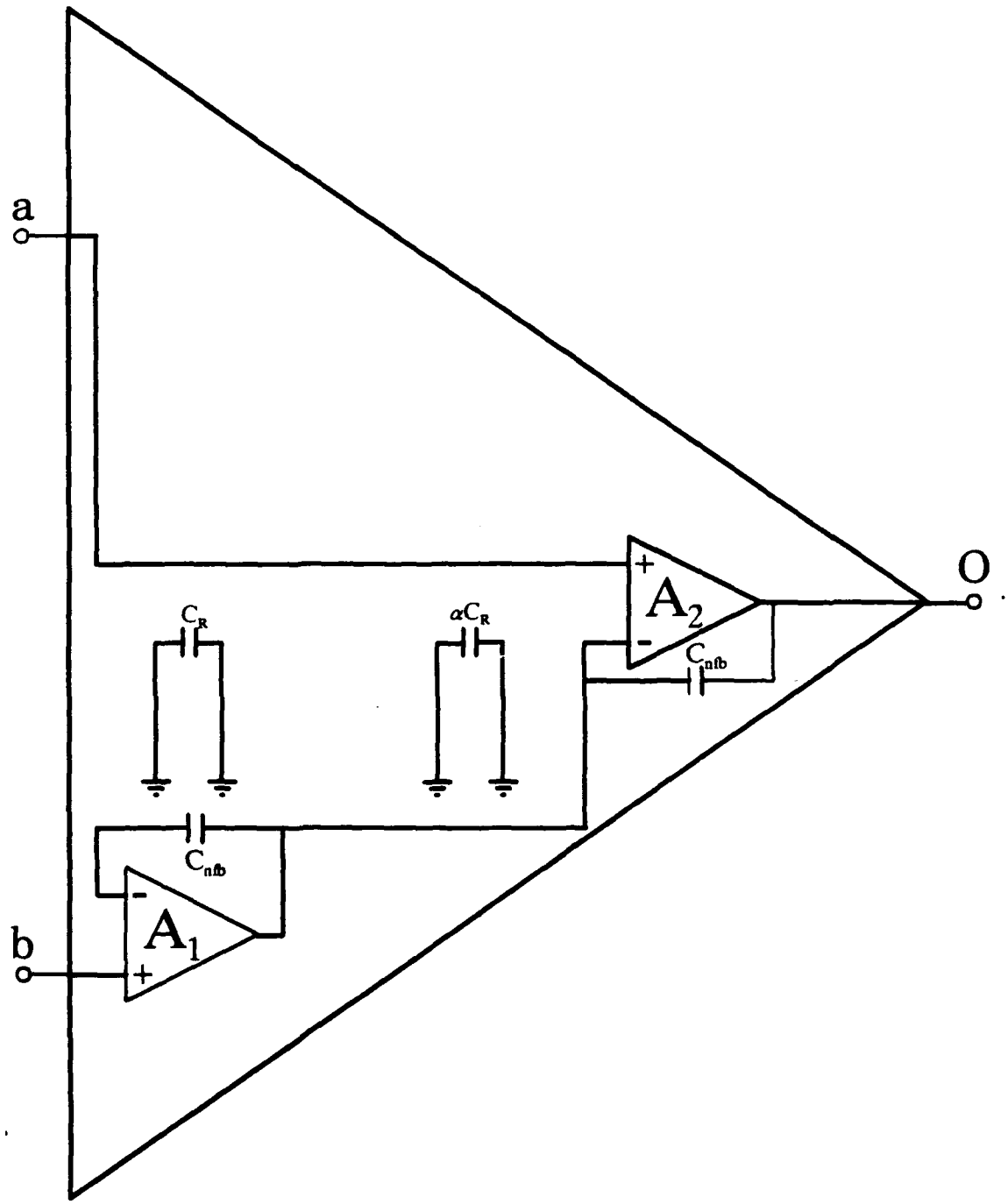

Figure 6.3i MOFR C2OA-1 with Φ_e Active and Effective Stray Capacitances

10. Stray Insensitive MOFR C2OA-1

Figure 6.3j depicts the final mOFR C2OA-1 circuit. This circuit will be implemented as the third design in this thesis. This circuit is missing only the two phase nonoverlapping clock design for completeness, but the actual design for this clock was shown in Chapter IV. The wiring diagram for this circuit as well as the wiring diagram for the two phase nonoverlapping clock will be shown in Chapter VII.

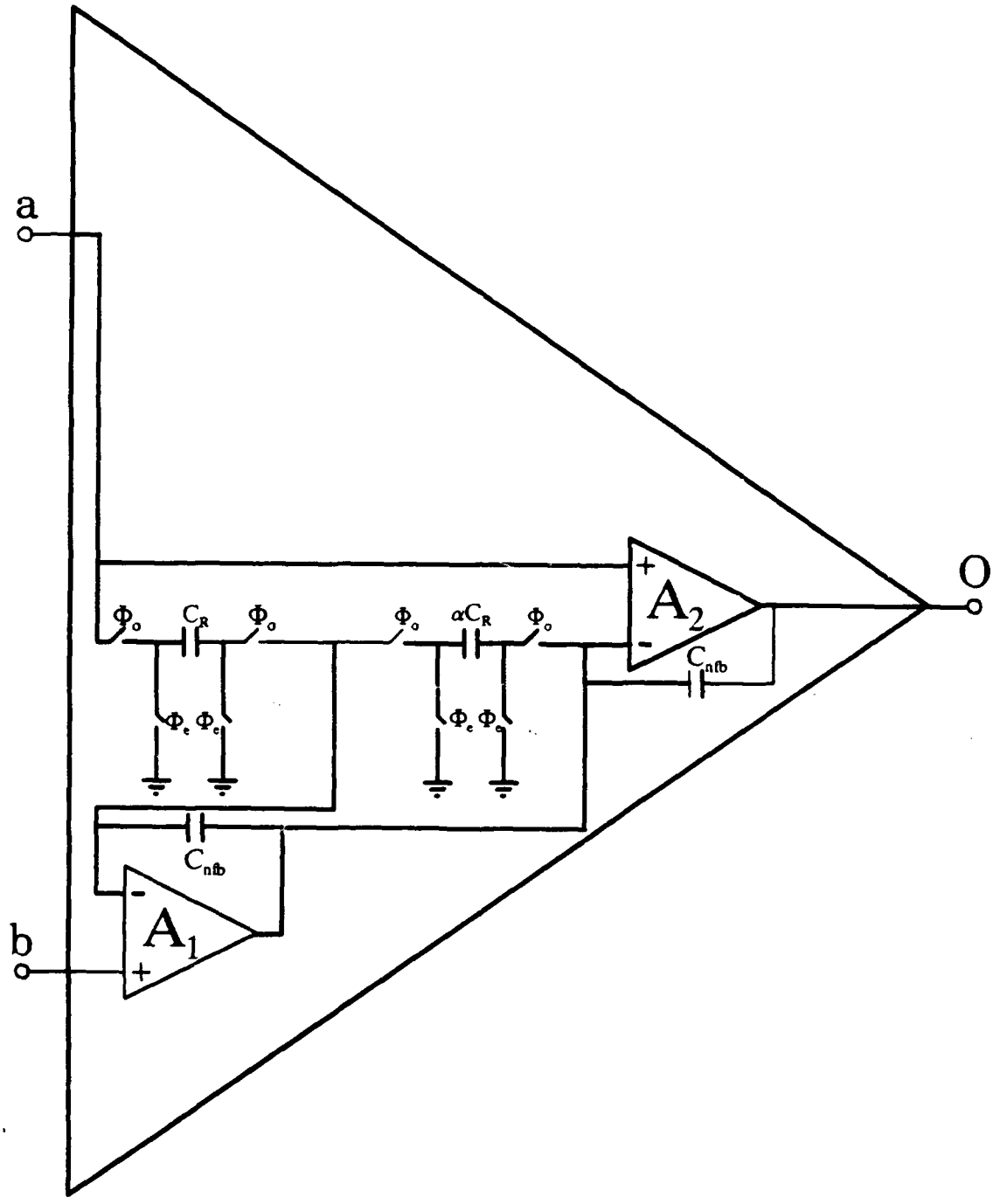

Figure 6.3j Stray Insensitive MOFR C2OA-1

E. MODIFIED OPEN-CIRCUIT FLOATING RESISTOR C2OA-2

1. C2OA-2

Figure 6.4a on the next page depicts C2OA-2 in its original form as designed from nullator and norator modeling and having passed the four required performance criteria as set forth in Chapter III. The three-terminal equivalent is shown to the upper right.

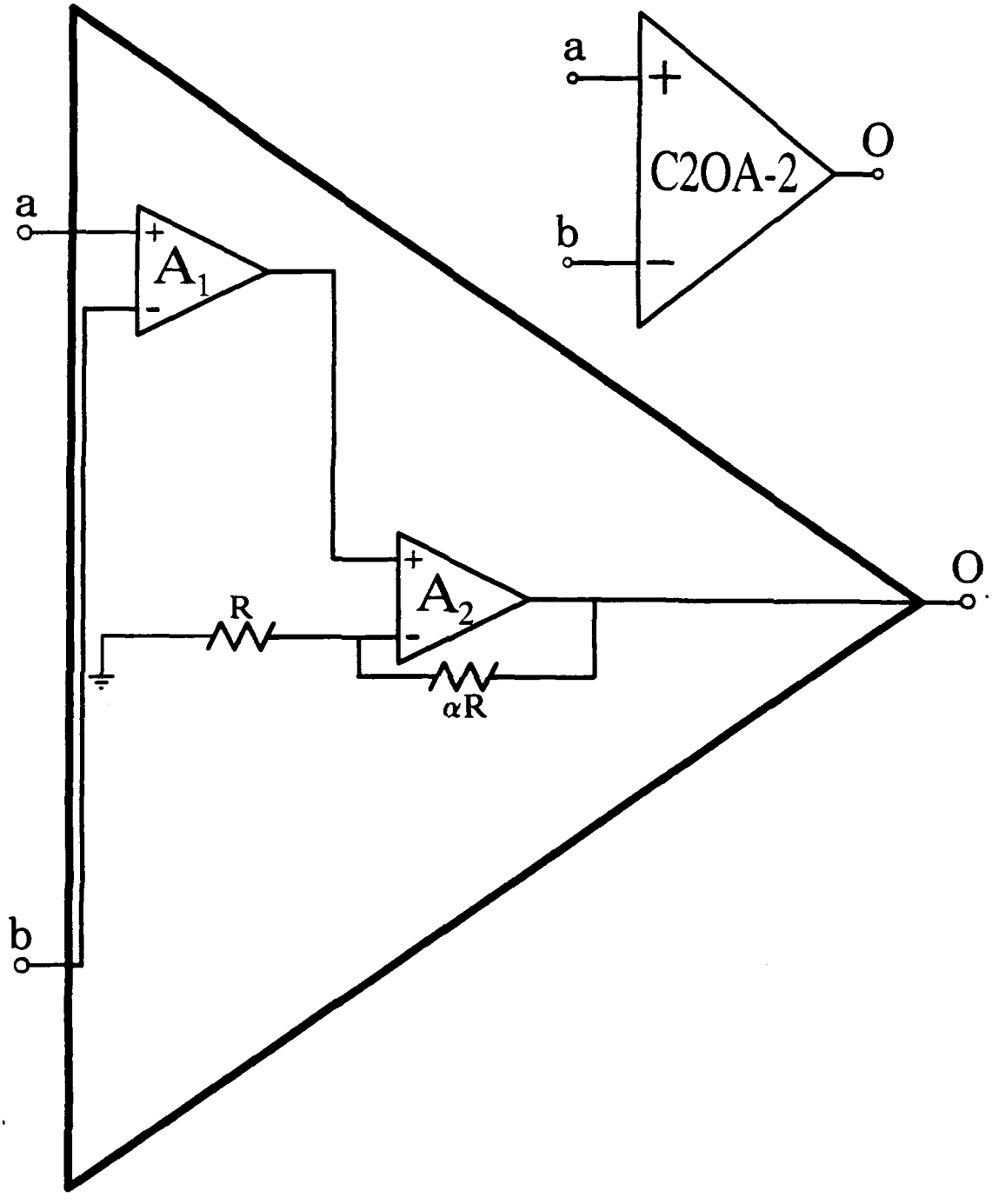

Figure 6.4a C2OA-2

2. MOFR C2OA-2

Figure 6.4b realizes the modified open-circuit floating resistor equivalent for the two resistors from the basic C2OA-2 form. Chapter IV detailed this transformation. In order to avoid nonlinearities and saturation, two capacitors, labeled C_{nfb}, were added.

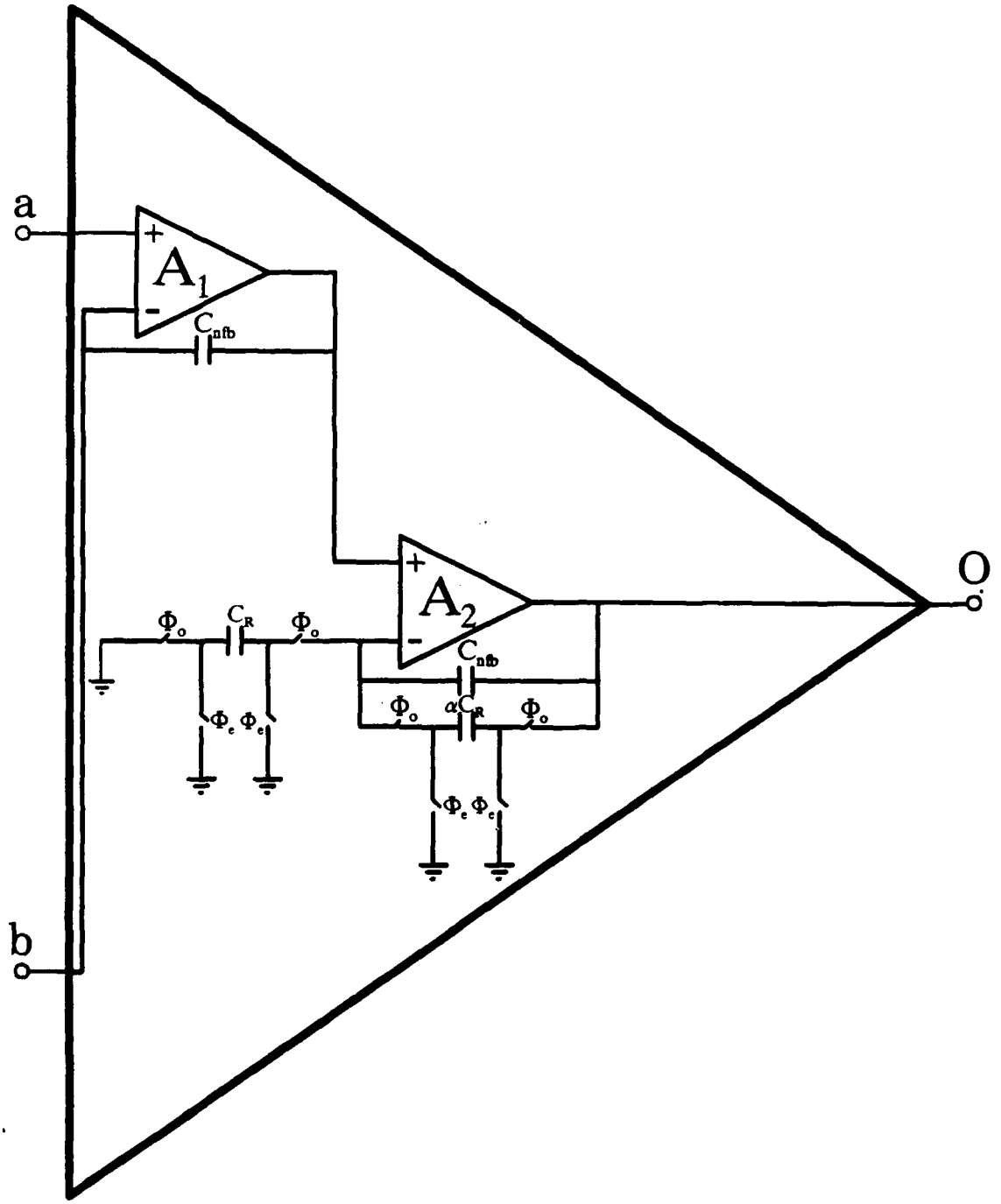

Figure 6.4b MOFR C2OA-2

3. MOFR C2OA-2 with Stray Capacitances

Figure 6.4c reflects the design with all possible stray capacitances added to the circuit as discussed in Chapter V. Not all of these stray capacitances actually exist, nor will all of them remain in the circuit if the design is well made. A good switched capacitor design will remove most, if not all, of the stray capacitances that were artificially introduced in the design.

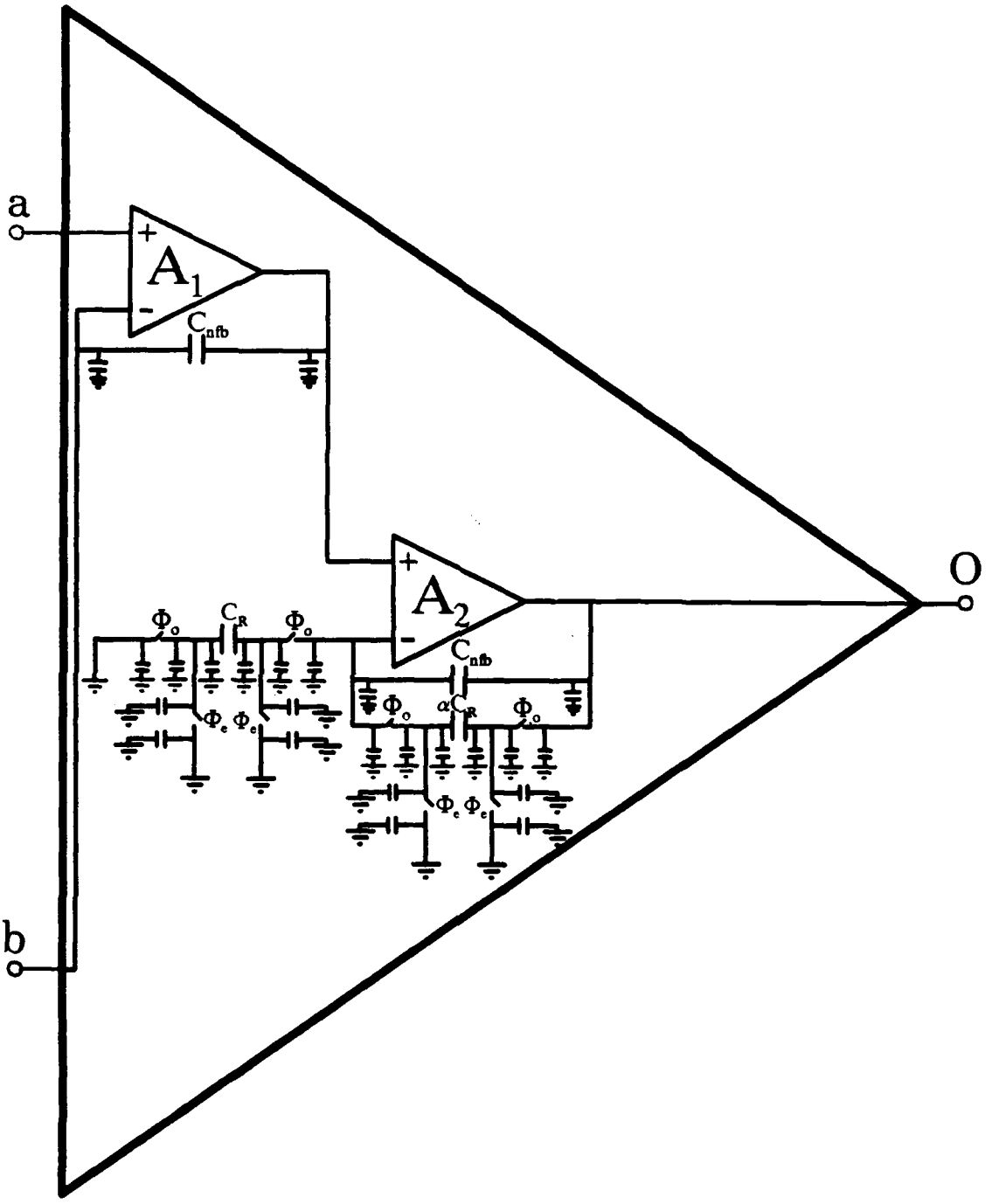

Figure 6.4c MOFR C2OA-2 with Stray Capacitances

4. MOFR C2OA-2 with Combined Stray Capacitances

Figure 6.4d combines the stray capacitances at each node into a single stray capacitance in order to simplify the circuit. The combined capacitors have been placed in the figure at a different position than any of the uncombined capacitors previously held so that they might present themselves more readily.

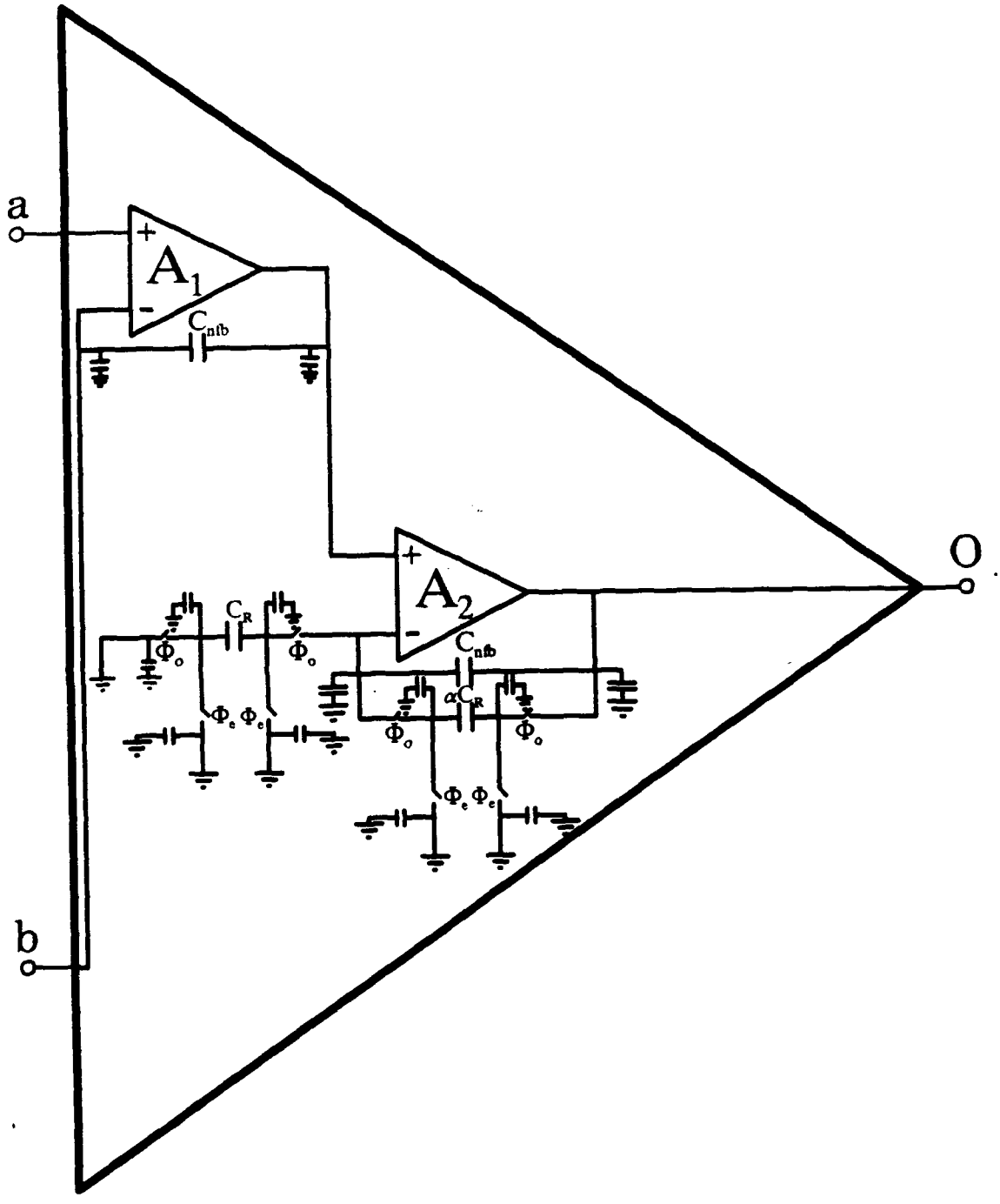

Figure 6.4d MOFR C2OA-2 with Combined Stray Capacitances

5. MOFR C2OA-2 with Reduced Stray Capacitances

Figure 6.4e removes some of the stray capacitances from the design. This reduction in stray capacitances was detailed in Chapter V and is summarized below:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.
2. Capacitances between the output of an OA and ground are inconsequential.
3. Capacitances that are driven by a voltage source are inconsequential.

The remaining stray capacitances are not necessarily effective stray capacitances. The mOFR topology must first be allowed to further reduce these parasitic capacitances.

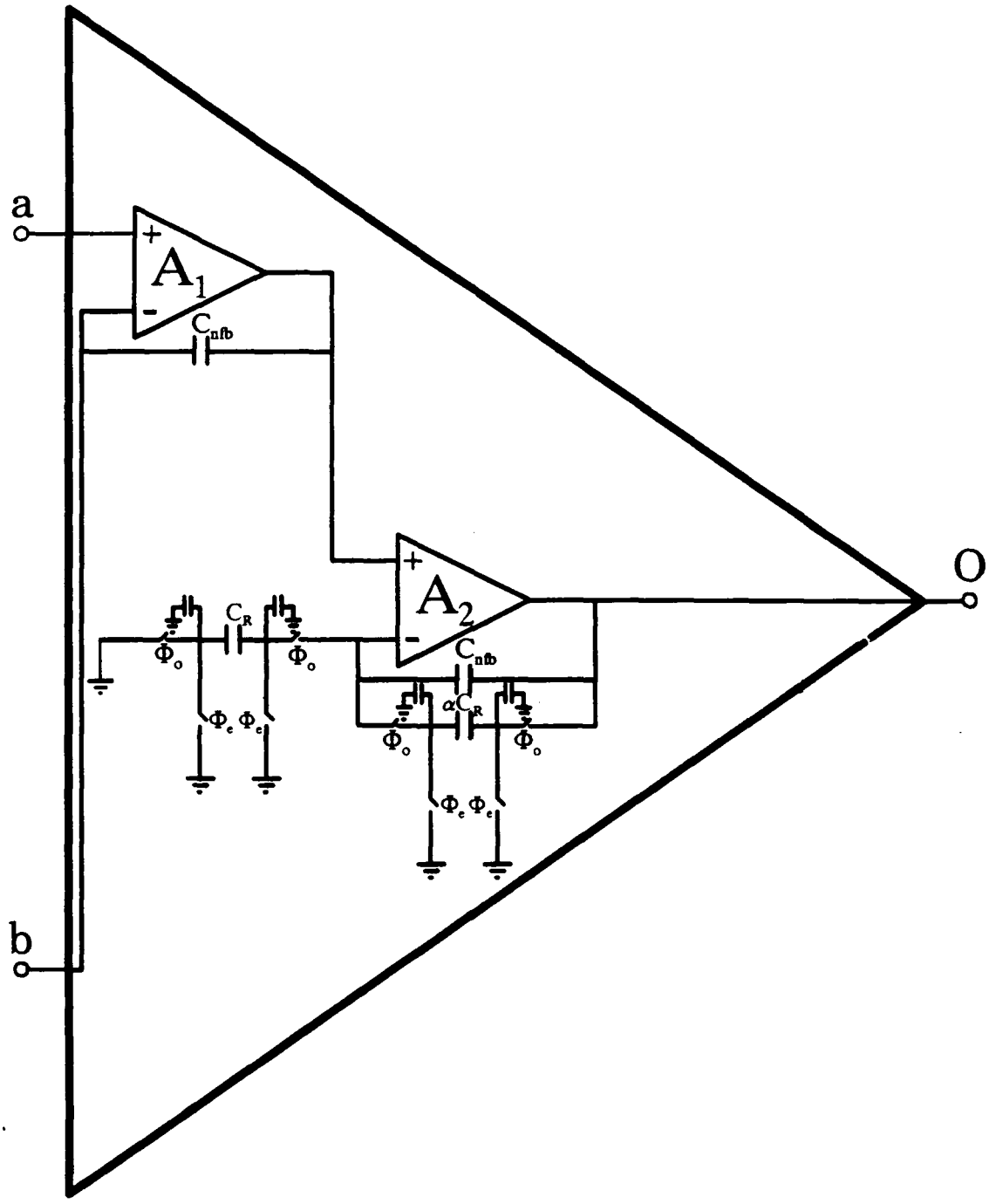

Figure 6.4e MOFR C2OA-2 with Reduced Stray Capacitances

6. MOFR C2OA-2 with Odd Phase Active

Figure 6.4f has the Φ_o clock active. This closes the four Φ_o switches and leaves the four Φ_e switches open and eliminates some of the circuit's complexity. The goal here is to ascertain which stray capacitances, if any, can be eliminated.

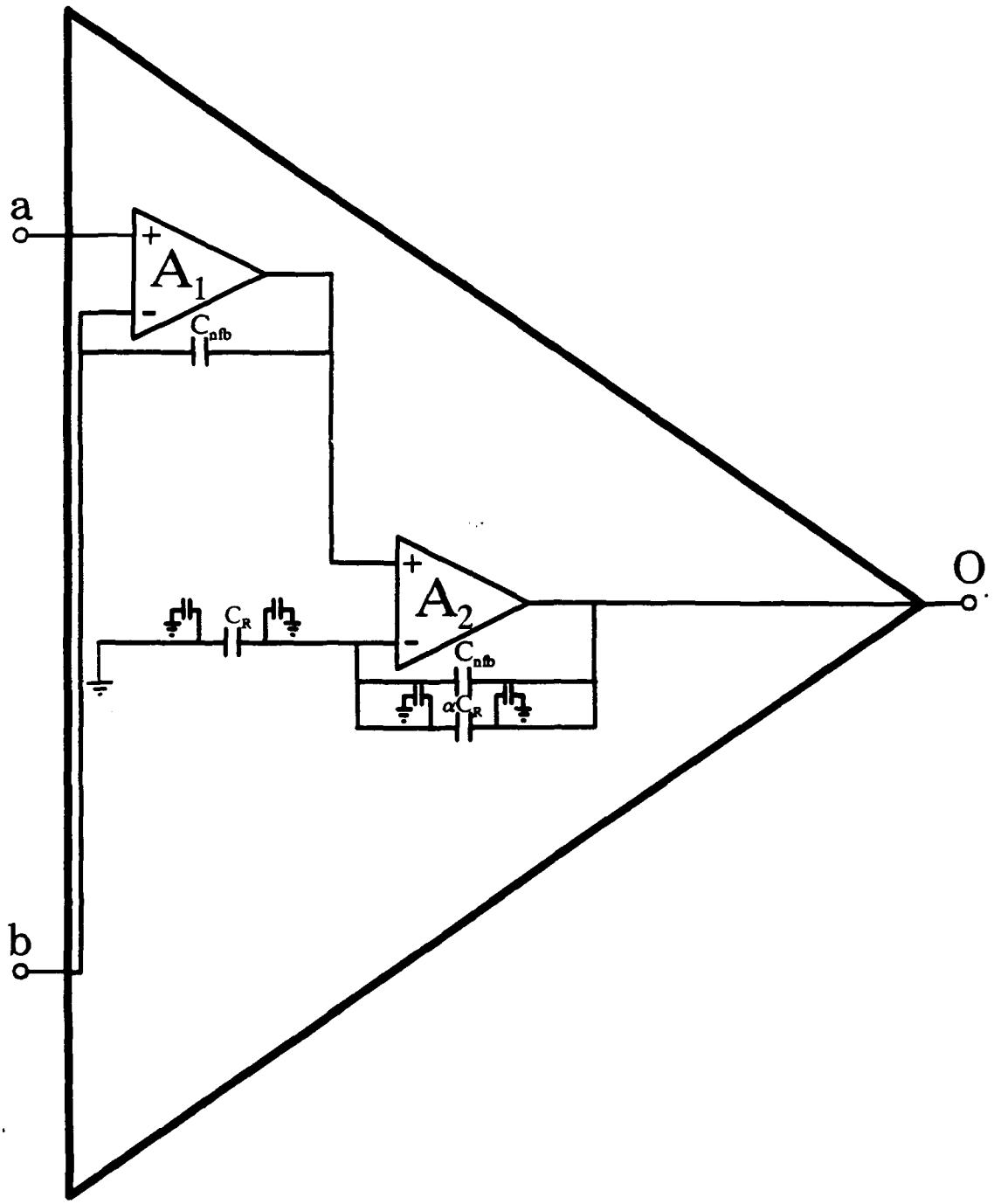

Figure 6.4f MOFR C2OA-2 with Odd Phase Active

7. MOFR C2OA-2 with Φ_o Active and Effective Stray Capacitances

Figure 6.4g removes some of the stray capacitances from the design. This reduction in stray capacitances leaves only the effective stray capacitances with the Φ_o clock active. This reduction in stray capacitances uses the familiar criteria:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.
2. Capacitances between the output of an OA and ground are inconsequential.
3. Capacitances that are driven by a voltage source are inconsequential.

In this particular case, all stray capacitances that originated from the modified open-circuit floating resistor implementation of C2OA-2 have been eliminated. These stray capacitances that were eliminated from the stray capacitances Φ_o clocked circuit will only be eliminated from the entire mOFR C2OA-2 circuit if they can additionally be eliminated from the Φ_e clocked circuit.

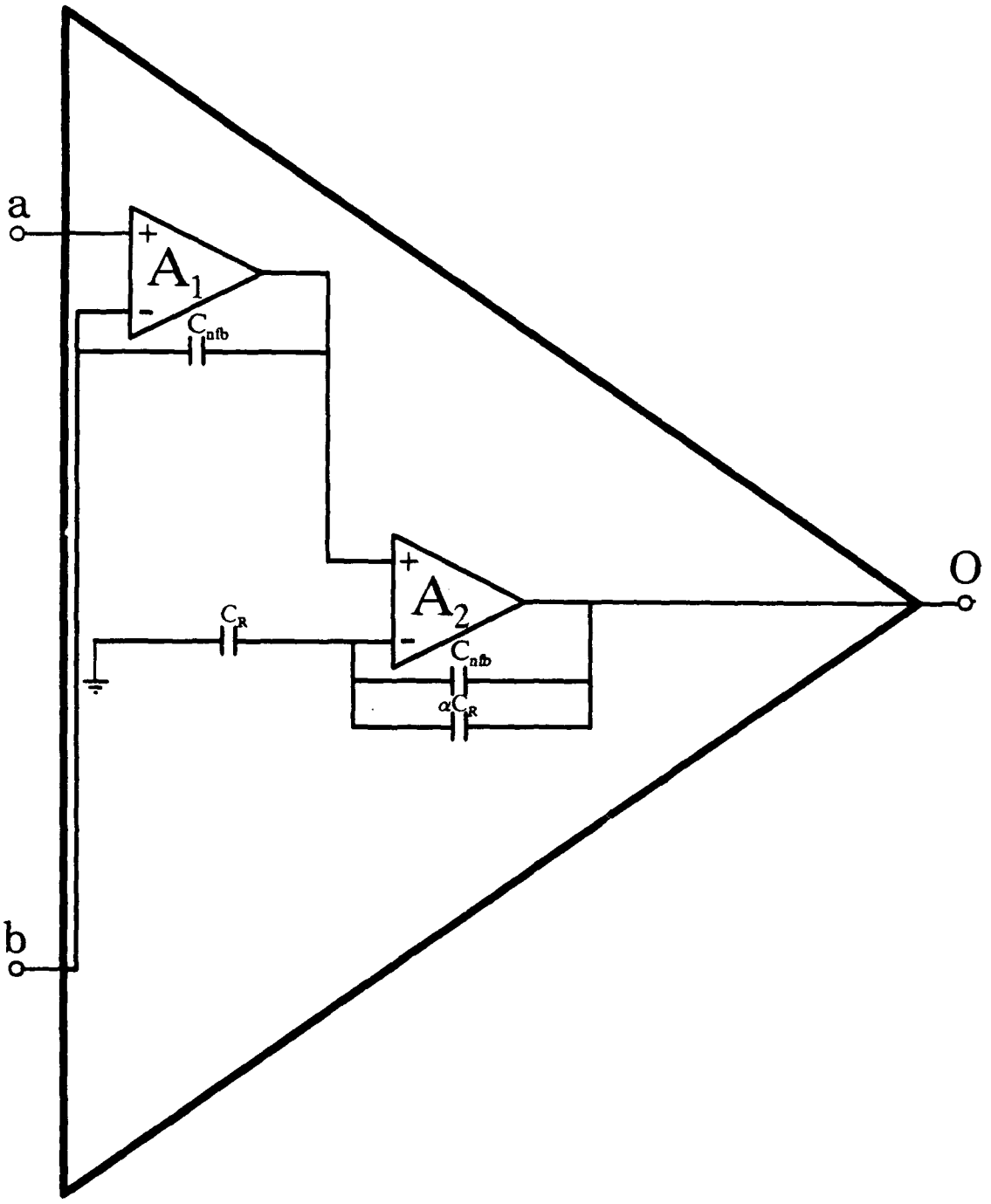

Figure 6.4g MOFR C2OA-2 with Φ_o Active and Effective Stray Capacitances

8. MOFR C2OA-2 with Even Phase Active

Figure 6.4h has the Φ_e clock active. This closes the four Φ_e switches and leaves the four Φ_o switches open and eliminates some of the circuit's complexity. The goal here is to ascertain which stray capacitances, if any, can be eliminated.

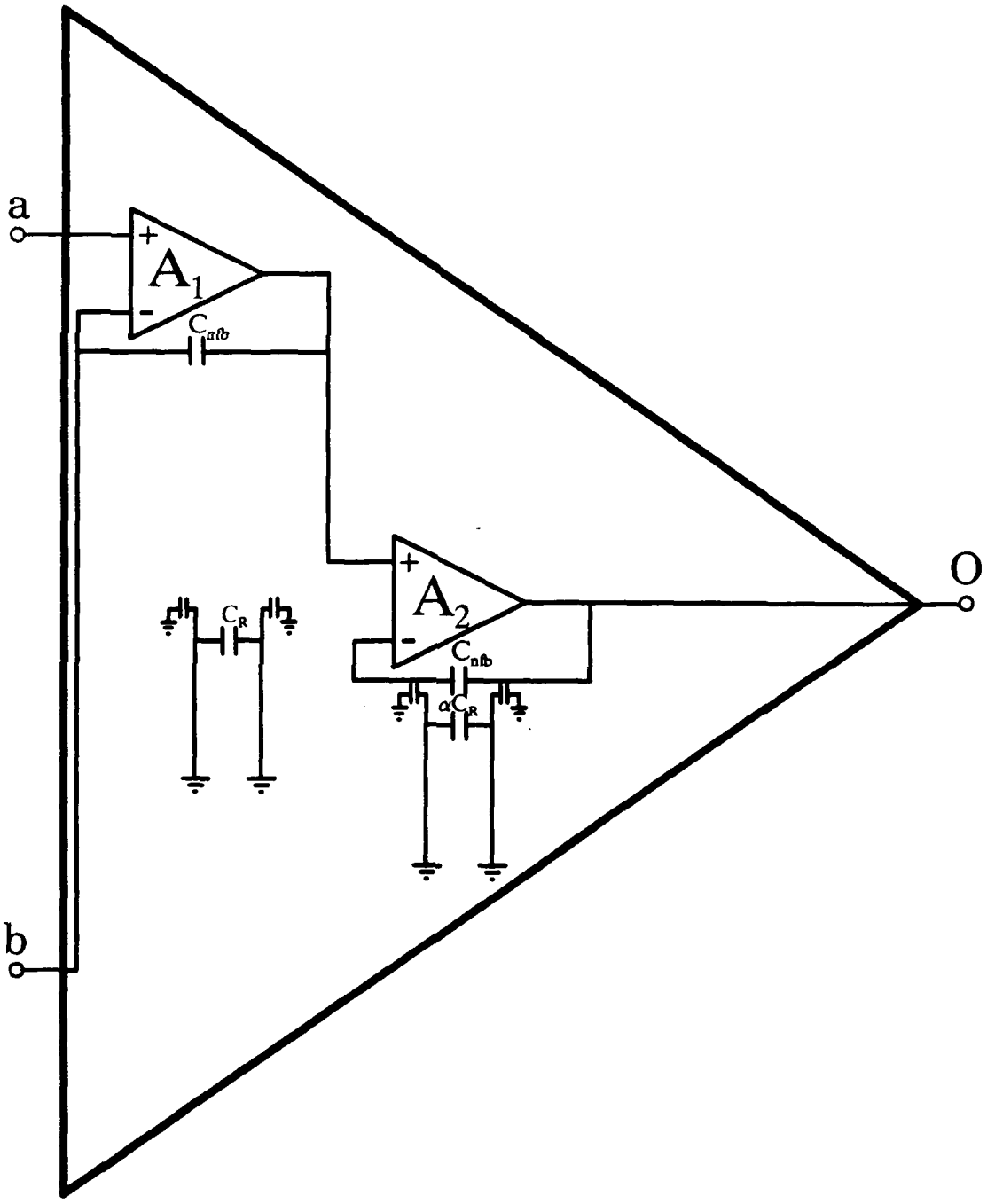

Figure 6.4h MOFR C2OA-2 with Even Phase Active

9. MOFR C2OA-2 with Φ_e Active and Effective Stray Capacitances

Figure 6.4i removes some of the stray capacitances from the design. This reduction in stray capacitances leaves only the effective stray capacitances with the Φ_e clock active. This reduction in stray capacitances uses the familiar criteria:

1. Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.
2. Capacitances between the output of an OA and ground are inconsequential.
3. Capacitances that are driven by a voltage source are inconsequential.

In this particular case, all stray capacitances that originated from the modified open-circuit floating resistor implementation of C2OA-2 have been eliminated. These stray capacitances that were eliminated from the stray capacitances Φ_e clocked circuit will be eliminated from the entire mOFR C2OA-2 circuit because they were previously eliminated from the Φ_o clocked circuit.

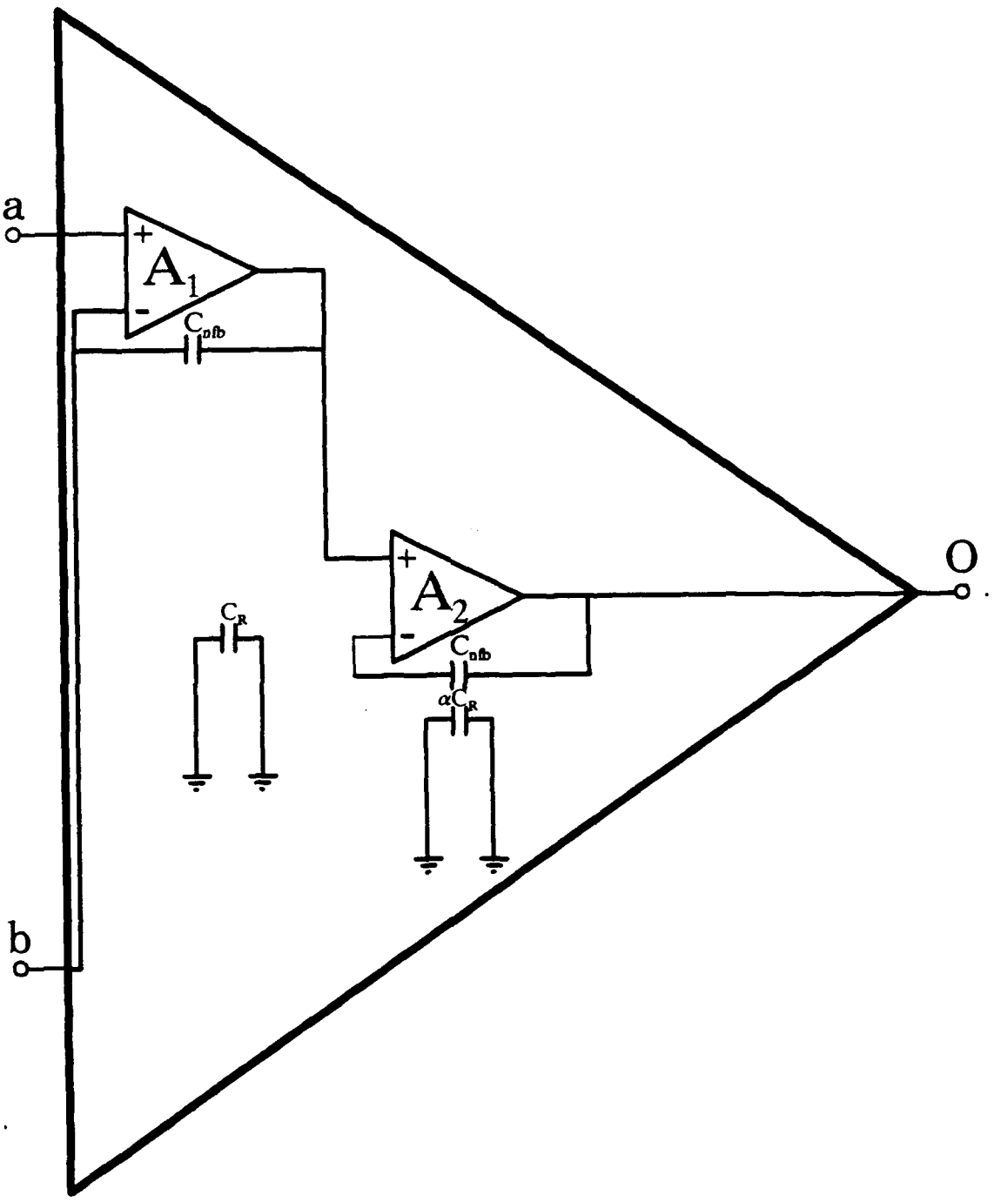

Figure 6.4i MOFR C2OA-2 with Φ, Active and Effective Stray Capacitances

10. Stray Insensitive MOFR C2OA-2

Figure 6.4j depicts the final mOFR C2OA-2 circuit. This circuit will be implemented as the third design in this thesis. This circuit is missing only the two phase nonoverlapping clock design for completeness, but the actual design for this clock was shown in Chapter IV. The wiring diagram for this circuit as well as the wiring diagram for the two phase nonoverlapping clock will be shown in Chapter VII.

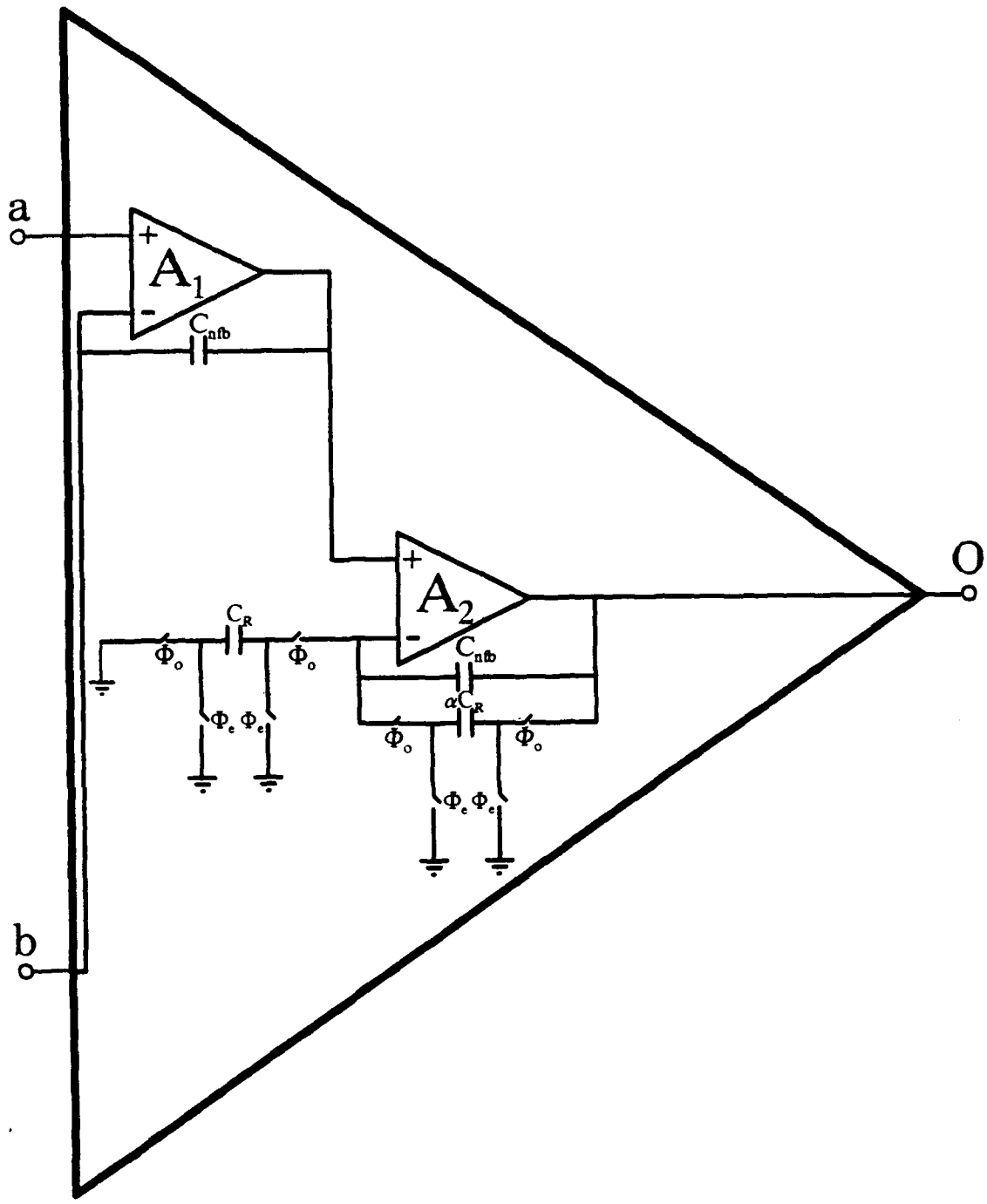

Figure 6.4j Stray Insensitive MOFR C2OA-2

VII. EXPERIMENTAL IMPLEMENTATION AND RESULTS

A. DESIGN IMPLEMENTATION

The four stray insensitive switched capacitor composite operational amplifier networks developed in Chapter VI will be implemented into a finite-gain configuration as shown in Figure 7.1 below.

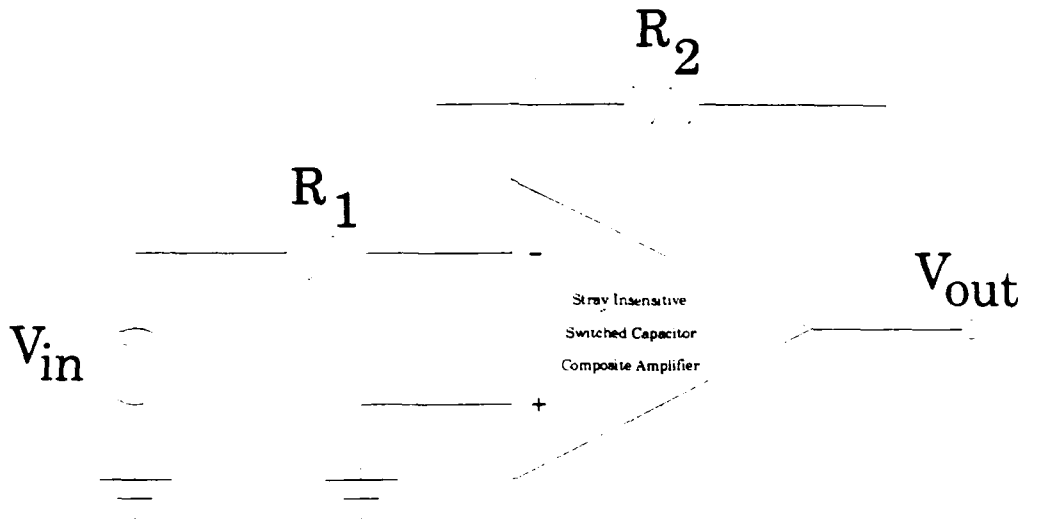

Figure 7.1 Finite-Gain Configuration

The wiring diagrams for the four stray insensitive switched capacitor composite operational amplifiers are shown in Figures 7.2, 7.3, 7.4, and 7.5 on the next four pages.

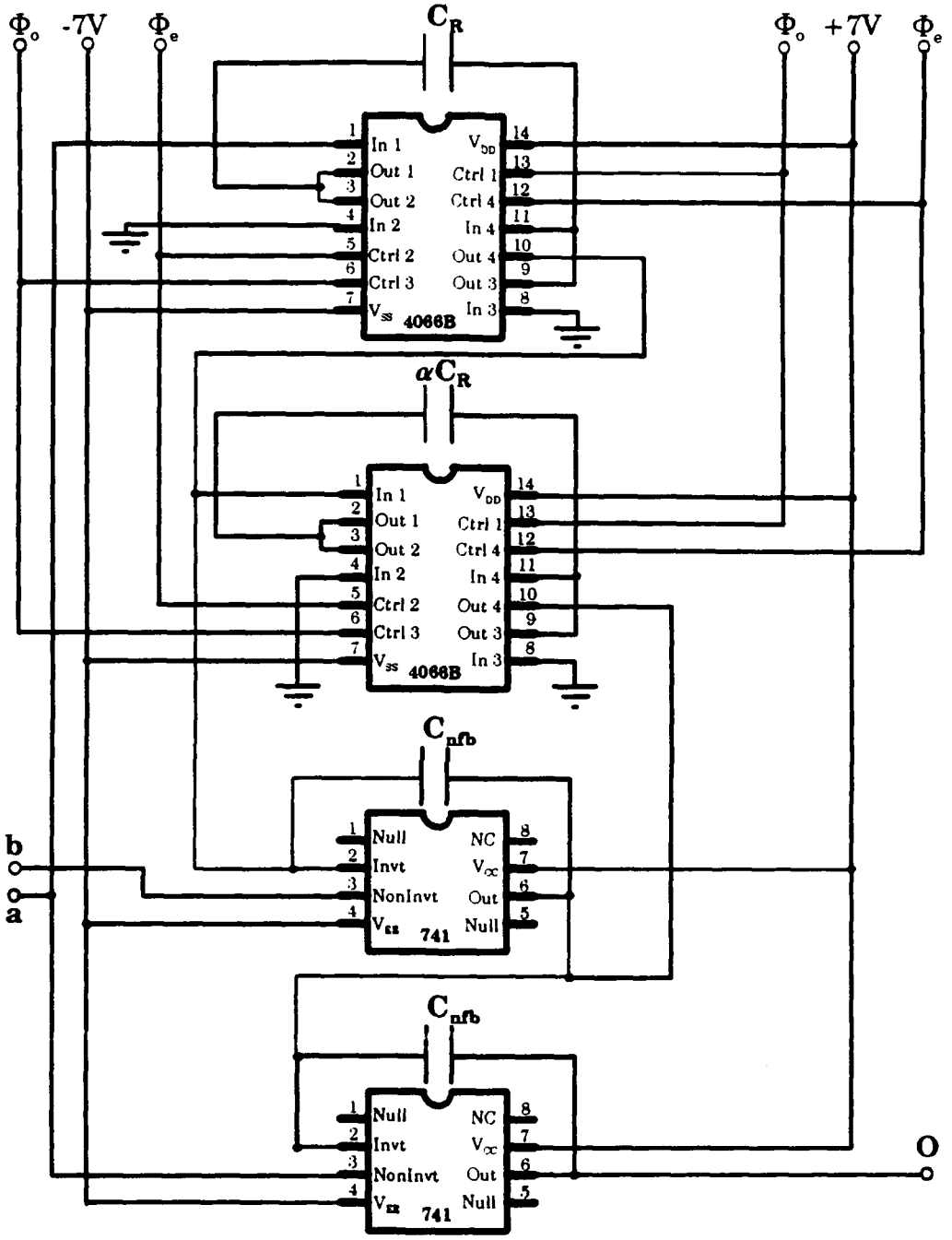

Figure 7.2 Stray Insensitive Toggle Switched Capacitor C2OA-1

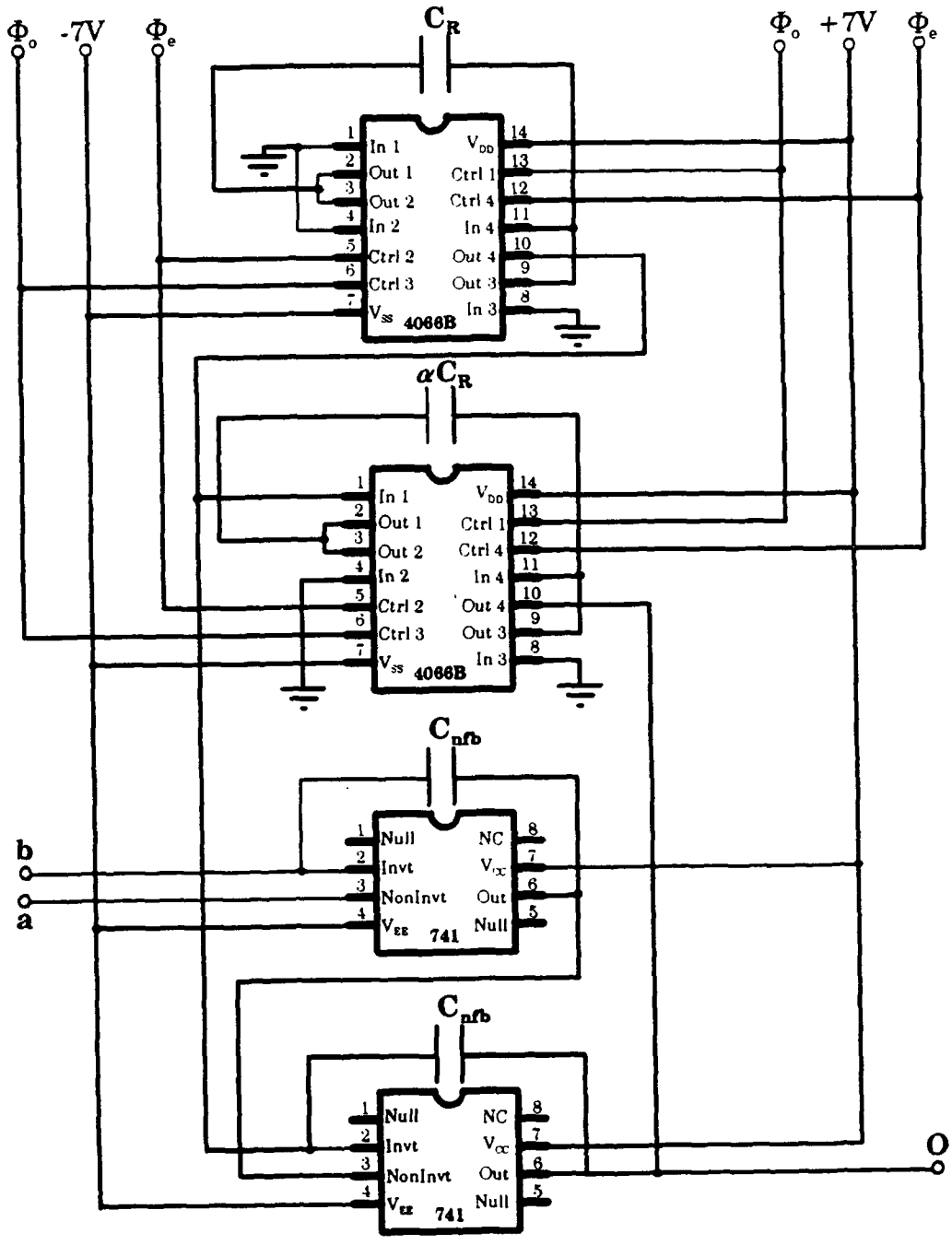

Figure 7.3 Stray Insensitive Toggle Switched Capacitor C2OA-2

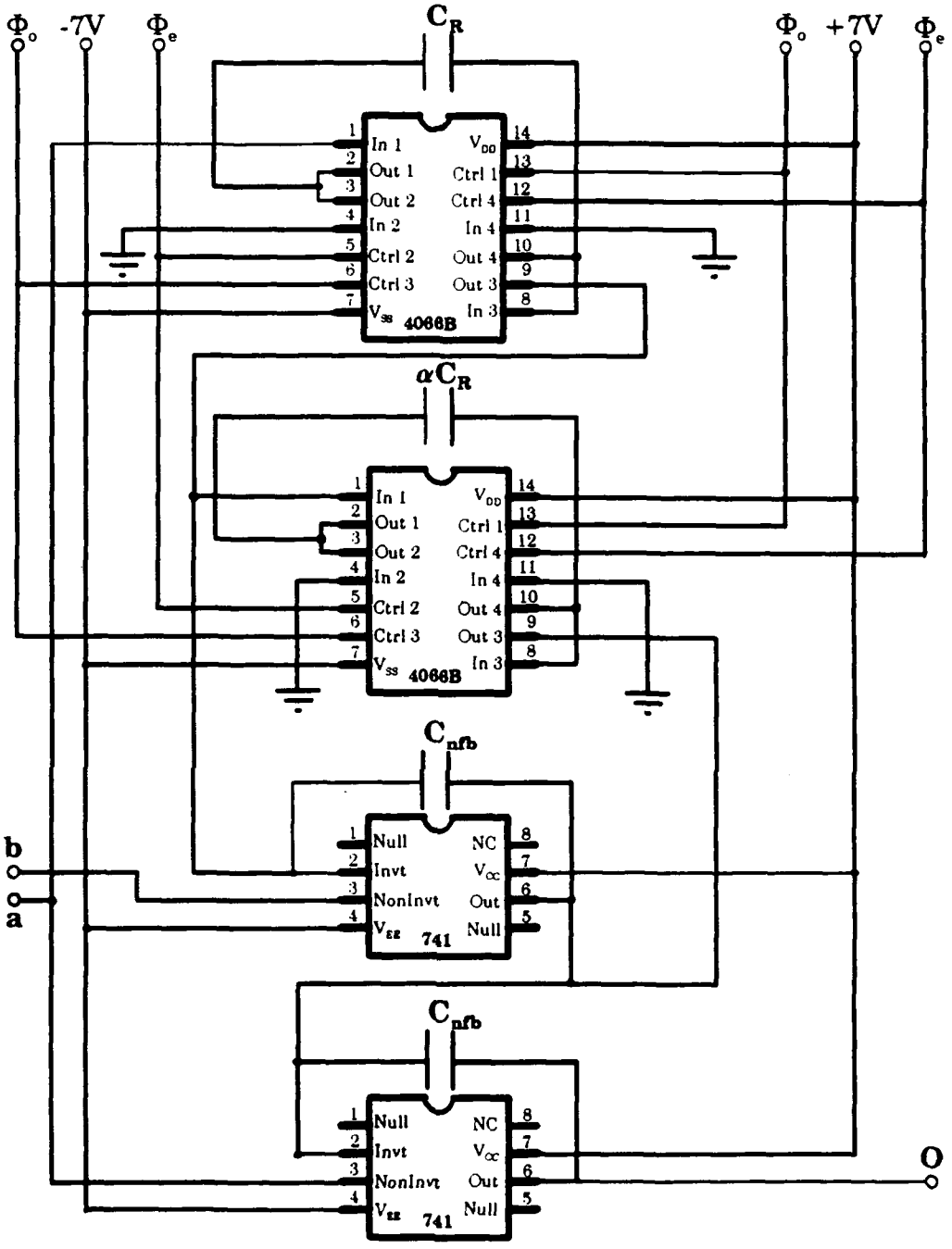

Figure 7.4 Stray Insensitive Modified Open-Circuit Floating Resistor C2OA-1

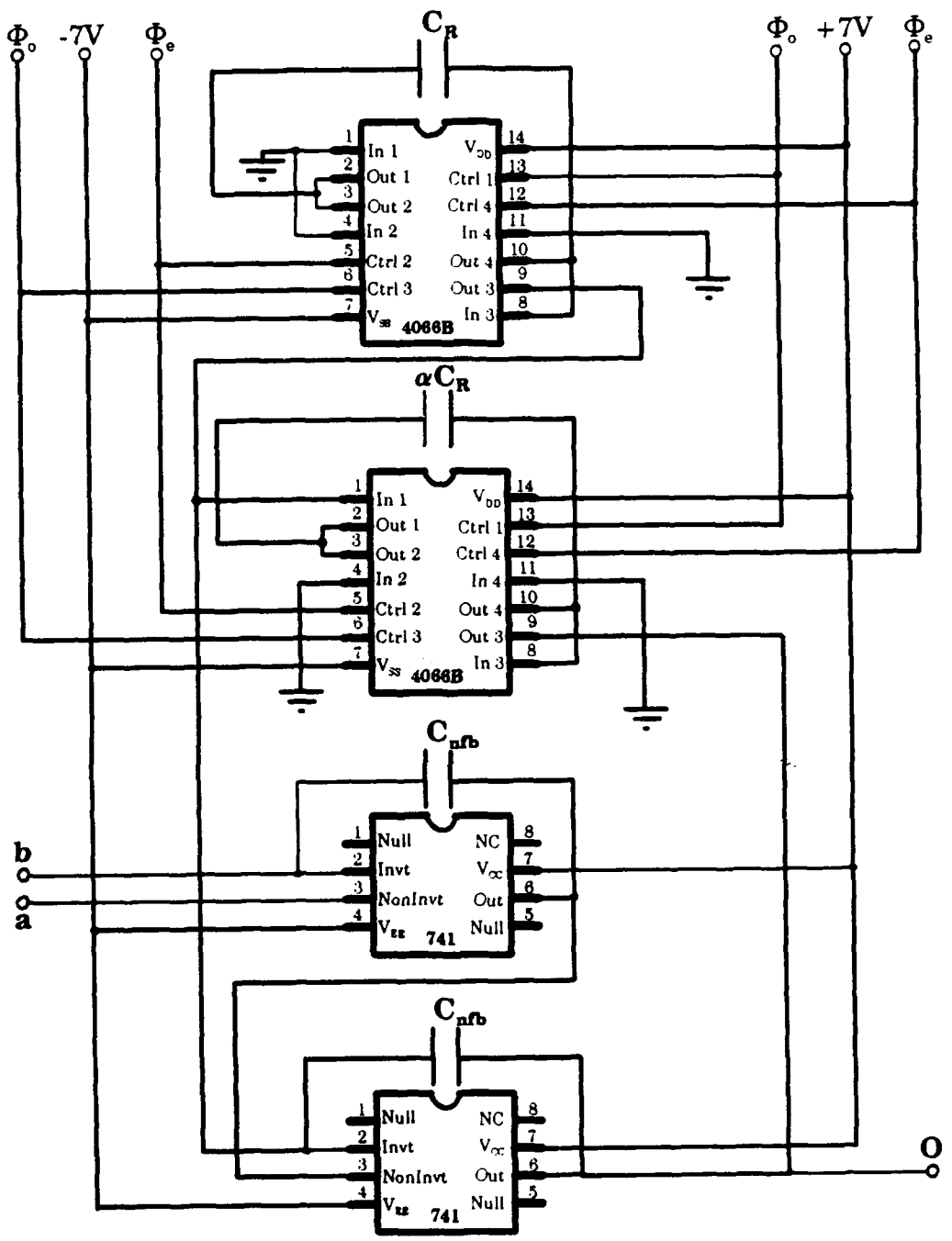

Figure 7.5 Stray Insensitive Modified Open-Circuit Floating Resistor C2OA-2

The wiring diagram for the two phase nonoverlapping clock is shown in Figure 7.6 below.

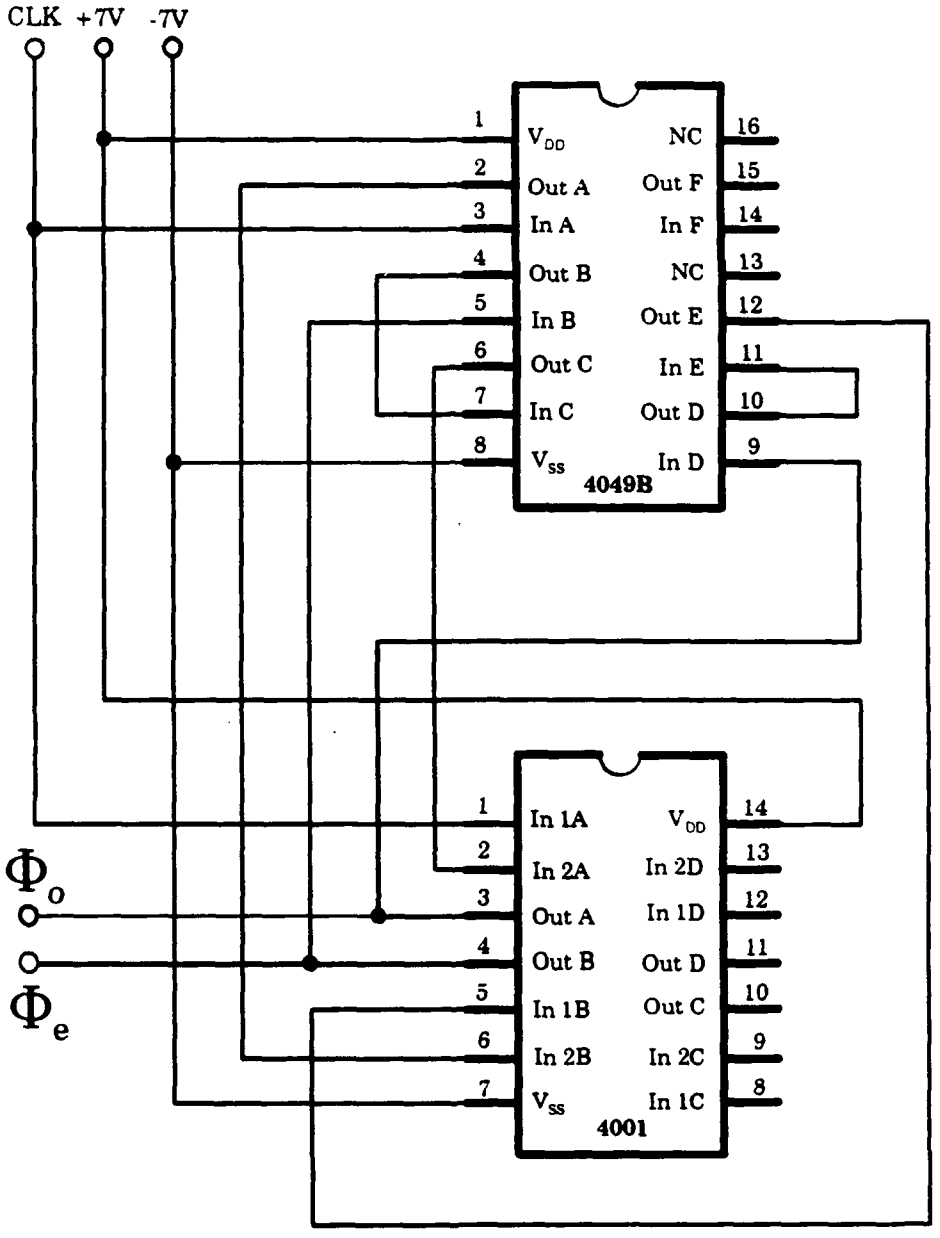

Figure 7.6 Two Phase Nonoverlapping Clock

B. THEORETICAL VALUES

In order to implement the stray insensitive networks the following theoretical values must be determined:

1. Finite-Gain Resistors, R_1 and R_2.
2. Quality Factor, Q.
3. Capacitor Ratio, α.
4. Switched Capacitor Equivalent Resistance, C_R.
5. Power Supply Voltage, V_{DD} or V_{CC} and V_{SS} or V_{EE}.
6. Negative Feedback Capacitors, C_{nfb}.
7. Input Signal Frequency, f_s.
8. Clock Frequency, f_c.

1. Finite-Gain Resistor Values

The finite-gain circuit used to test the four networks will have a gain of 100 with R_1 = 1 kΩ and R_2 = 100 kΩ. This gain of 100 will allow for practical testing and verification of the design. Using a gain of 10 would increase the bandwidth to approximately 100 kHz for the single OAs and to approximately 300 kHz for the composite OAs. In order to avoid warping this would require a clock frequency of no less than 3 MHz, however, as we will see shortly, the clock frequency is limited to less than 2 MHz by the settling time of the OAs. Increasing the gain to 1000 would decrease the bandwidth to approximately 1 kHz for single OAs and to approximately 30 kHz for

composite OAs but the very high gain will require an impractical small input signal level with very low signal to noise ratio

2. Quality Factor

A quality factor of 0 7071 is used so that a maximally flat gain response will be observed.

3. Capacitor Ratio

For C2OA-1, a theoretical value for α is determined using Equation 3 5 which is repeated here

$$Q_p = \frac{(1+\alpha)}{\sqrt{(1+k)}} \sqrt{\frac{\omega_2}{\omega_1}} \qquad (7.1)$$

In this thesis, the gain bandwidth product, ω_1, for op amp A_1, is equal to the gain bandwidth product, ω_2, for op amp A_2, because both op amp A_1 and op amp A_2 are LM741 op amps. Solving for α we now have

$$\alpha = Q_p \sqrt{1 + k} - 1 \qquad (7.2)$$

Since Q_p and k are known we conclude that

$$\alpha = 0.7071 \sqrt{(1 + 100)} - 1 \cong 6.1 \qquad (7.3)$$

For C2OA-2, a theoretical value for α is determined using Equation 3.9 which is repeated here

$$Q_p = \frac{(1+\alpha)}{\sqrt{(1+k)}} \sqrt{\frac{\omega_1}{\omega_2}} \qquad (7.4)$$

and using the same arguments as before, α was also found to be equal to 6.1

4. Switched Capacitor Equivalent Resistance

Now that α has been determined to be equal to 6.1, finding values for C_R and αC_R is easy. C_R was chosen to be 1000 pF and αC_R was forced to be 6100 pF. A 1000 pF capacitor was chosen as the base element size due to the accuracy with which it was made. 100 pF capacitors were only accurate to within 5 % of stated value and capacitors of 1000 pF were accurate to within 2 % of stated value.

5. Power Supply Voltage

Power supply voltage should be made as large as possible in order to allow for a large signal to noise ratio (SNR). The quad bilateral switch, the 4066B chip, used in this thesis has a maximum voltage range of $\pm$ 7.5 V_{PEAK}. This was the most limiting of the chips used in the design, in fact, it cut the SNR in half. The power supply voltage was chosen to be $\pm$ 7.0 V.

6. Negative Feedback Capacitors

The feedback capacitor values are anticipated to be small since they are equivalent to a large resistor value. The exact value will have to be found experimentally. The feedback capacitor is used to avoid nonlinearities and saturation. It is anticipated

that capacitors in the tens of pF range will suffice. The circuits were initially wired in using feedback capacitors of 100 pF. By using 100 pF feedback capacitors, the circuits, as designed, will operate, as is. Final values for the feedback capacitors can be obtained by experimentation. Inserting smaller and smaller valued capacitors (equivalent to larger and larger feedback resistance) until the design no longer behaves properly and then increasing the value slightly.

7. Input Signal Frequency

The input signal frequency was initially chosen to be a sinusoid of 1 kHz, however, the oscilloscopes used to test the circuits did not produce acceptable output at that frequency. Synchronization was a problem and the signal could not be "locked" and could only be seen in a flickering state at best. The input frequency was then increased to 10 kHz and the problems were gone. The amplitude of the input frequency is not as easily found. Slew rate and its associated problems must be keep at the forefront of our minds in determining an acceptable amplitude. Slew rate is defined as the maximum rate of change of voltage that can accurately be followed by the op amp, or

$$SR = \left.\frac{dv_o}{dt}\right|_{max} \tag{7.5}$$

Let's define our input signal to be

$$v_I = \hat{V}_{in} \sin\omega t \tag{7.6}$$

The rate of change of this input signal is

$$\frac{dv_I}{dt} = \omega \hat{V}_{in} \cos\omega t \tag{7.7}$$

The largest value that this rate of change could become is

$$\left.\frac{dv_I}{dt}\right|_{\max} = \omega_M \hat{V}_{in} \tag{7.8}$$

Thus, the slew rate equation would become

$$SR = \omega_M \hat{V}_{outmax} \tag{7.9}$$

where

$$\hat{V}_{outmax} = \hat{V}_{in} k \tag{7.10}$$

and k is the closed-loop gain. Rearranging Equation 7 9 we find that the maximum input frequency allowed is

$$\omega_M = \frac{SR}{\hat{V}_{outmax}} \tag{7.11}$$

or, in hertz, our full power bandwidth is

$$f_M = \frac{SR}{2\pi \hat{V}_{outmax}} \tag{7.12}$$

Now substituting in the input voltage and the closed-loop gain we have

$$f_M = \frac{SR}{2\pi k \hat{V}_{in}} \tag{7.13}$$

Solving for the input voltage amplitude gives us

$$\hat{V}_{inmax} = \frac{SR}{2\pi k f_M} \tag{7.14}$$

Using typical values for the LM 741 op amp and a very conservatively computed maximum expected frequency of 100 kHz, we find,

$$\hat{V}_{inmax} = \frac{0.5V / \mu sec}{2\pi(100)(100kHz)} = 8\ mV \tag{7.15}$$

Equation 7.15 limits our input signal amplitude to 8 mV. As an extra precaution and to make finding the 3 dB point easier, an input signal amplitude of 7 mV was chosen. The anticipated output voltage will then be 700 mV and the 3 dB voltage will approximately be equal to 500 mV (a voltage that is easy to see on an oscilloscope).

Initially, an input voltage of 7 mV_{pp} was used. The input voltage was then varied between 5 mV_{pp} and 10 mV_{pp} to test the BW and the theoretical input voltage limit. The bandwidths for all seven circuits did not change with this limited input signal variation.

Input signals above 10 mV_{pp} did change the bandwidth of the circuits. An input signal above 10 mV_{pp} caused slew rate error in the circuits. This 10 mV_{pp} limit closely matches the theoretical limit of 8 mV_{pp}.

It is difficult to see slew rate error on the oscilloscope when using signals in this frequency range and magnitude. The only certain way would be to use a spectrum analyzer to detect nonlinearity, which would show a single peak if the slew rate range was not exceeded and multiple peaks, at the odd harmonics, if nonlinearity occurs and the slew rate forced the sinusoid into a triangular waveform.

8. Clock Frequency

The clock frequency had to be no less than twice the input signal frequency or the Nyquist Rate for sampling would not have been followed and aliasing would have ensued. In order to prevent warping, the clock frequency had to be at least ten times the input frequency. The settling time for OAs vary between manufacturer even for the LM741, however, they all have a settling time of 0.5 μsec (or better) and this forces the clock frequency to be less than 2 MHz. Based on these values a sinusoidal clock of 1MHz with an amplitude of 14 V_{pp} was chosen. The amplitude of 14 V_{pp} was determined by the power supply voltage limitation of the 4066B chip (quad bilateral switch) previously mentioned in the power supply subsection.

C. EXPERIMENTAL RESULTS

Table 7.1 contains the measured experimental results. Seven designs are listed. The first three designs are the reference designs built using continuous resistors and are used only as a tool for making comparisons. The last four designs are the stray insensitive switched capacitor networks that were developed throughout this thesis. All entries in Table 7.1 are measured values.

Table 7.1 EXPERIMENTAL RESULTS

Design	R_2 / R_1	α	3dB BW
Single LM 741	99.90	-N/A-	8.57 kHz
Continuous C2OA-1	100.25	6.09	90.00 kHz
Continuous C2OA-2	98.70	6.29	90.00 kHz
Stray Insensitive TSC C2OA-1	99.10	5.80	121.43 kHz
Stray Insensitive TSC C2OA-2	99.59	5.93	90.00 kHz
Stray Insensitive mOFR C2OA-1	98.40	5.88	88.00 kHz
Stray Insensitive mOFR C2OA-2	98.80	5.79	88.00 kHz

The theoretical value for finite-gain was 100 and the actual values fair favorably The theoretical value for α was 6.1 and the actual values come fairly close The theoretical 3 dB BW for the single OA was 9.9 kHz [Ref. 8:p. 117] and the actual value was within experimental limits. The theoretical value for the 3 dB BW for the composite amplifiers is $[(\sqrt{k})$(3 dB BW single OA)] or 99 kHz, where k = 100 The 3 dB bandwidths for the composite amplifiers are well within tolerance.

The 3 dB bandwidth for the TSC C2OA-1 was above the theoretical value and yet it is not an unrealistic value considering that the finite-gain is 100. Extra care was taken to ensure that slew rate was not exceeded for that design and several different input signal amplitudes were used ranging from 5 mV_{pp} to 10 mV_{pp} and the bandwidth did not change. Extending the amplitude above 10 mV_{pp}, however, showed signs of slew rate error and eventually saturation.

Noise and clock feed through were apparent in the output waveforms, however, they were not a factor. A 1μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor inserted between V_{DD} and ground and between V_{SS} and ground reduced noise levels significantly. No output filtering was needed to produce sharp signals.

All four designs had some output offset voltage present. The C2OA-1s required input voltage biasing on op amp A_2 and the C2OA-2s required input biasing on op amp A_1. Input voltage biasing was performed using a potentiometer across pins 1 and 5, the op amp null offset pins; the variable resistance pin of the potentiometer was wired into either V_{DD} or V_{SS} as required.

The composite amplifiers are stable by design. Internally, neither op amp requires any additional feedback to maintain stability and linearity as these requirements were imposed in their design using the four performance criteria. The switched capacitor implementation of these composite op amps placed an unswitched capacitor across each of these op amps. An attempt was made to remove these unswitched capacitors.

The unswitched capacitor in parallel with the switched capacitor, as shown in Figure 6.2j and Figure 6.4j cannot be removed. These unswitched capacitors prevent the op amp from going into an open-loop configuration as discussed in Chapter V and as detailed in Reference 11. The removal of these capacitors did, in fact, destroy the circuit integrity.

The following unswitched capacitors can be removed without any performance degradation. The C2OA-1 design does not need the negative feedback capacitor, shown in Figure 6.1j and Figure 6.3j, around op amp A_2. The C2OA-2 design does not need the negative feedback capacitor, shown in Figure 6.2j and Figure 6.4j, around op amp A_1.

VIII. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE RESEARCH

A. CONCLUSIONS

The four stray insensitive switched capacitor networks designed in this thesis have shown that a practical implementation of the switched capacitor is possible. Their parasitic free operation is accomplished using stray insensitive topologies. These four designs show great promise in filtering and the stray insensitive switched capacitor composite amplifier has all the prerequisites for making a superior building block for an A/D converter.

B. RECOMMENDATIONS FOR FUTURE RESEARCH

The four stray insensitive switched capacitor composite operational amplifiers designed in this thesis need to be implemented onto a single IC so that their inherent advantages can be used in various applications, not the least of which would be filtering.

A more rigorous project would be to rework the original composite operational amplifier designs. The four C20A-*i* designs of 1981 had to pass performance criteria that did not include using switched capacitor techniques and stray insensitive topologies that might have made more than four designs stand out from the rest. In particular, the original nullator-norator pairing did not have the switched capacitor's ability to implement negative resistance. The switched capacitor's ability to implement negative resistance should open up the Pandora's box of circuit design.

LIST OF REFERENCES

1. Michael, S. N., *Composite Operational Amplifiers and Their Application in Active Networks*. Ph.D. Dissertation, West Virginia University, Morgantown, West Virginia, August 1983

2. Mikhael, W. B., and Michael, S., "Composite Operational Amplifiers: Generation and Finite-Gain Applications," *IEEE Transactions on Circuits and Systems*, v. CAS-34, No. 5, pp. 449-460, May 1987

3. Mikhael, W. B., and Michael, S., "Inverting Integrator and Active Filter Applications of Composite Operational Amplifiers," *IEEE Transactions on Circuits and Systems*, v.CAS-34, No. 5, pp. 461-470, May 1987.

4. Mikhael, W. B., and Michael, S., "A Systematic General Approach for the Generation of Composite OAs with some Useful Applications in Linear Active Networks," in *Proceedings of the 25th Midwest Symposium on Circuits and Systems*, pp. 454-463, Houghton, Michigan, August 1982.

5. Mikhael, W. B., and Michael, S., "High-Speed, High Accuracy Integrated Operational Amplifiers," *Proceedings of the Midwest Symposium on Circuits and Systems*, Morgantown, West Virginia, June 1984.

6. Michael, S. N., and Mikhael, W. B., "Generation of Actively Compensated Composite Operational Amplifiers and Their use in Extending the Operational Frequencies of Linear Active Networks," *Proceedings of the IEEE Symposium on Circuits and Systems*, Newport Beach, California, May 1983.

7. Mikhael, W. B., and Michael, S., "Actively Compensated Composite Operational Amplifiers," *Proceedings of the Midwest Symposium on Circuits and Systems*, Albuquerque, New Mexico, June 1981.

8. Sedra, A. S., and Smith, K. C., *Microelectronic Circuits*, 2d ed., Holt, Rinehart and Winston, Inc., 1987.

9. Raisor, R. C., *Parasitic Free Switched Capacitor Composite Operational Amplifiers*, Master's Thesis, Naval Postgraduate School, Monterey, California, June 1991

10. Kollomorgan, G. S., *Generation of Programmable Composite Operational Amplifiers with a CMOS Integrated Circuit.* Master's Thesis, Naval Postgraduate School, Monterey, California, December 1986.

11. Schaumann, R. S., Ghuasi, M. S., and Laker, K. R., *Design of Analog Filters Passive. Active RC. and Switched Capacitor.* Prentice Hall, 1990.

BIBLIOGRAPHY

Ghausi, M. S., Laker, K. R., *Modern Filter Design Active RC and Switched Capacitor.* Prentice Hall, 1981.

Gregorian, R., and Temes, G. C., *Analog MOS Integrated Circuits for Signal Processing.* John Wiley & Sons, 1986.

Horowitz, P., and Hill, W., *The Art of Electronics.* 2d ed., Cambridge University Press, 1989.

Sage, E. S., *Total Dose Radiation Effects on Bipolar Composite and Single Operational Amplifiers Using a 30 MEV Linear Accelerator.* Master's Thesis, Naval Postgraduate School, Monterey, California, June 1988.

Yalkin, C., *Digitally Programmable Active Switched Capacitor Filters.* Master's Thesis, Naval Postgraduate School, Monterey, California March 1987.

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